PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H01J 63/02, 9/26

A1

(11) International Publication Number: WO 94/18694

(43) International Publication Date: 18 August 1994 (18.08.94)

(21) International Application Number: PCT/US94/00602

(22) International Filing Date: 1 February 1994 (01.02.94)

(30) Priority Data:

012,542	1 February 1993 (01.02.93)	US
188,857	31 January 1994 (31.01.94)	US
188,856	31 January 1994 (31.01.94)	US

(71) Applicant: SILICON VIDEO CORPORATION [US/US]; 10460 Bubb Road, Cupertino, CA 95014 (US).

(72) Inventors: FAHLEN, Theodore, S.; 6131 Courta De La Reina, San Jose, CA 95120 (US). DUBOC, Robert, M., Jr.; 300 Santa Rita Avenue, Menlo Park, CA 94025 (US). CURTIN, Christopher, J.; 11022 Canyon Vista Drive, Cupertino, CA 95014 (US). SPINDT, Christopher, J.; 115 Hilside Avenue, Menlo Park, CA 94025 (US). LOVOI, Paul, A.; 19152 Dehavilland Drive, Saratoga, CA 95070 (US). NOWICKI, Ronald, S.; 722 Kenley Way, Sunnyvale, CA 94087 (US). MORRIS, David, L.; 3644 El Grande Court, San Jose, CA 95132 (US). SCHMID, Anthony, P.; 461 Canyon Drive, Solana Beach, CA 92075 (US).

(74) Agents: MEETIN, Ronald, J. et al.; Skjerven, Morrill, MacPherson, Franklin & Friel, Suite 700, 25 Metro Drive, San Jose, CA 95110 (US).

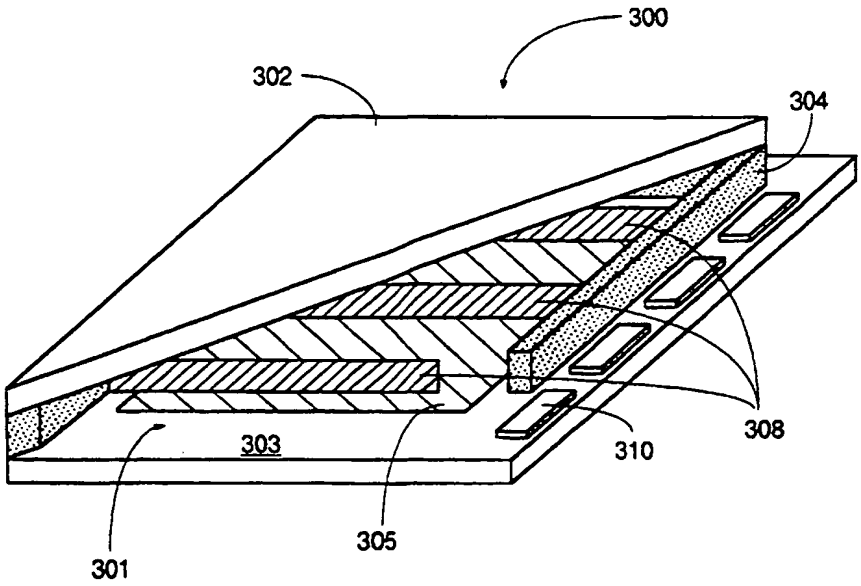
(81) Designated States: AT, AU, BB, BG, BR, BY, CA, CH, CZ, DE, DK, ES, FI, GB, HU, JP, KP, KR, KZ, LK, LU, MG, MN, MW, NL, NO, NZ, PL, PT, RO, RU, SD, SE, SK, UA, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published

With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: FLAT PANEL DEVICE WITH INTERNAL SUPPORT STRUCTURE AND/OR RAISED BLACK MATRIX



(57) Abstract

A flat panel device (300) includes a spacer (308) for providing internal support. The spacer can be made of ceramic or glass-ceramic. Spacer surfaces exposed within the flat panel device are treated to reduce secondary emissions and prevent charging of the spacer surfaces. A light-emitting structure contains a main section (302), a pattern of dark ridges (314) situated along the main section, and a plurality of electron-activated light-emissive regions (313) situated in spaces between the ridges. The dark ridges extend further away from the main section than the light-emissive regions to form a raised black matrix. When the light-emitting structure is used in an optical display, the raised black matrix contacts spacers (308) and, in so doing, protects the light-emissive regions from being damaged. The light-emitting structure can be formed according to various techniques of the invention.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgystan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

FLAT PANEL DEVICE WITH INTERNAL SUPPORT STRUCTURE AND/OR RAISED BLACK MATRIX

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to flat panel devices such as flat cathode ray tube (CRT) displays. This invention also relates to techniques used in fabricating flat panel devices.

2. Related Art

Numerous attempts have been made in recent years to construct a flat CRT display (also known as a "flat panel display") to replace the conventional deflected-beam CRT display in order to provide a lighter and less bulky display. In addition to flat CRT displays, other flat panel displays, such as plasma displays, have also been developed.

In flat panel displays, a faceplate, a backplate, and connecting walls around the periphery of the faceplate and backplate form an enclosure. In some flat panel displays, the enclosure is held at vacuum pressure, e.g., in flat CRT displays, approximately 1×10^{-7} torr. The interior surface of the faceplate is coated with light emissive elements such as phosphor or phosphor patterns which define the active region of the display. The light emissive elements are caused to emit light, e.g., cathodic elements located adjacent the backplate are excited to release electrons which are accelerated toward the

phosphor on the faceplate, causing the phosphor to emit light which is seen by a viewer at the exterior surface of the faceplate (the "viewing surface").

During display operation, the electron-emissive elements are selectively excited to cause certain of the elements to emit electrons that move towards phosphors on the faceplate. These phosphors, upon being struck by the impinging electrons, emit light that is visible at the exterior surface of the faceplate.

The electrons emitted from each of the sets of electron-emissive elements are intended to strike only certain target phosphors. However, some of the emitted electrons invariably strike portions of the faceplate outside the target phosphors. To improve contrast at the faceplate, a matrix of dark non-reflective regions that emit substantially no light when struck by electrons from the electron-emissive elements are suitably dispersed among the phosphor regions. In a color display, this black matrix also improves color purity. The phosphor regions extend further away from the faceplate than the black matrix.

In vacuum pressure flat panel displays, a force is exerted on the walls of the flat panel display due to the differential pressure between the internal vacuum pressure and the external atmospheric pressure that, left unopposed, can make the flat panel display collapse. In rectangular displays having greater than an approximately 1 inch diagonal (the diagonal is the distance between opposite corners of the active region), the faceplate and backplate are particularly susceptible to this type of mechanical failure due to their high aspect ratio. Here, "aspect ratio" is defined as either the width, i.e., distance between the interior surfaces of opposing connecting walls, or the height, i.e., distance between the interior surface of the faceplate and the interior surface of the backplate, divided by the thickness. The faceplate or backplate of a flat panel display may also

fail due to external forces resulting from impacts sustained by the flat panel display.

Spacers have been used to internally support the faceplate and/or backplate. Previous spacers have been walls or posts located between pixels (phosphor regions that define the smallest individual picture element of the display) in the active region of the display.

Spacers have been formed by photopatterning polyimide. However, polyimide spacers have been found inadequate because of: 1) insufficient strength; 2) inability to match the coefficient of thermal expansion with the materials typically used for the faceplate (e.g., glass), backplate (e.g., glass, ceramic, glass-ceramic or metal) and addressing grid (e.g., glass-ceramic or ceramic), resulting in registration problems; and 3) outgassing that may occur when polyimide is used in a vacuum pressure environment.

Spacers have also been made of glass. However, glass may not have adequate strength. Further, micro-cracks that are inherent in glass make glass spacers even weaker than "ideal" glass because of the tendency of micro-cracks to propagate easily throughout glass.

Additionally, for any spacer material, the presence of the spacers may adversely affect the flow of electrons toward the faceplate in the vicinity of the spacer. For example, stray electrons may electrostatically charge the surface of the spacer, changing the voltage distribution near the spacer from the desired distribution and resulting in distortion of the electron flow, thereby causing distortions in the image produced by the display.

SUMMARY OF THE INVENTION

According to the invention, a flat panel device includes a spacer for providing internal support of the device. In particular, for devices which operate with an internal vacuum pressure, the spacer prevents the device from collapsing as a result of stresses arising from the

differential pressure between the internal vacuum pressure (i.e., any pressure less than atmospheric pressure) and the external atmospheric pressure. The spacer also internally supports the device against stresses arising from external impact forces. Additionally, surfaces of the spacer within the enclosure are treated to prevent or minimize charge buildup on the spacer surfaces. Consequently, the presence of the spacer does not adversely affect the flow of electrons near the spacer, so that the image produced by the device is not distorted.

In one embodiment of the invention, a coating is formed on spacer surfaces, the coating being a material having a secondary emission ratio δ less than 4 and a sheet resistance between 10^9 and 10^{14} ohms/□. In an additional embodiment, the coating has a secondary emission ratio δ less than 2. The coating is selected from a group of materials including chromium oxide, copper oxide, carbon, titanium oxide and vanadium oxide. In one particular embodiment, the coating is chromium oxide.

In another embodiment of the invention, a first coating is formed on spacer surfaces. A second coating is formed over the first coating. The first coating is a material having a sheet resistance between 10^9 and 10^{14} ohms/□. The second coating is a material having a secondary emission ratio δ less than 4. In an additional embodiment the second coating has a secondary emission ratio δ less than 2.

In yet another embodiment of the invention, spacer surfaces are first surface-doped to produce a sheet resistance between 10^9 and 10^{14} ohms/□, then a coating is formed over the doped spacer surfaces, the coating being a material having a secondary emission ratio δ less than 4. In an additional embodiment the coating has a secondary emission ratio δ less than 2. The coating is selected from a group of materials including chromium oxide, copper oxide, carbon, titanium oxide and vanadium oxide. In one particular embodiment, the coating is chromium oxide.

In still another embodiment, spacer surfaces are surface-doped to produce a sheet resistance between 10^9 and 10^{14} ohms/□.

In each of the above embodiments including a coating or coatings, the total thickness of the coating or coatings is between 0.05 and 20 μm. In the embodiment including two coatings, the coating having a secondary emission ratio δ less than 4 is preferably formed with a thickness between 0.01 and 0.05 μm. Preferably, the coating or coatings are formed such that the sheet resistance varies no more than ± 2% throughout the coating. In each of the embodiments in which spacer surfaces are surface-doped, the dopant can be, for instance, titanium, iron, manganese or chromium.

The spacer can be made of, for instance, ceramic and can be a spacer wall, a spacer structure, or some combination of a spacer wall, spacer walls, and spacer structure. The flat panel device also contains a mechanism to emit light. The flat panel device can include a field emitter cathode or a thermionic cathode. In alternative embodiments, the faceplate and backplate of the flat panel device can both be straight or both be curved. In a further embodiment of the invention, the flat panel device can include an addressing grid.

In an additional embodiment of the invention, one or more electrodes are formed on the treated spacer surfaces. For instance, an electrode can be formed near an interface of the spacer and backplate, the voltage of the electrode being controlled to achieve a desired voltage distribution in the vicinity of the interface, thereby deflecting the flow of electrons as desired to correct for distortions resulting from imperfections in the surface treatment or misalignment of the spacer. In a further embodiment, this electrode can be formed with a serpentine path with respect to an interior surface of the backplate in order to achieve a desired voltage distribution.

A voltage divider establishes the voltage of each electrode. In one embodiment, the voltage divider is a resistive coating formed on the spacer surfaces. The sheet resistance of the coating must be closely controlled (preferably ± 2%) to achieve accurate voltages on the electrodes. In another embodiment, the voltage divider can be a resistive strip that is positioned outside the enclosure across the electrically conductive traces that extend from each of the electrodes. The voltage control of the voltage divider can be fine-tuned by "trimming," i.e., selectively removing material from the voltage divider to vary local resistance to establish the desired voltages on the electrodes.

In a further embodiment of the invention, a strip of electrically conductive material ("edge metallization") is formed between an edge surface of the spacer and the backplate, and in intimate contact with the entire length of the spacer. If a resistive coating is formed on the spacer surfaces, the edge metallization is electrically connected to the resistive coating. In that case, the edge metallization and the resistive coating are formed such that an interface between the edge metallization and the resistive coating is at a constant distance from an interior surface of the backplate. In like manner, edge metallization is formed between an edge surface of the spacer and the faceplate to establish good electrical connection between the faceplate and spacer.

In a method according to the invention, a flat panel device is assembled by mounting a spacer between a backplate and faceplate, treating surfaces of the spacer to prevent or minimize charge buildup on the spacer surfaces, coating an edge surface of the spacer with edge metallization such that the edge metallization forms an electrical connection between the spacer and backplate, and sealing the backplate and faceplate together to encase the spacer in an enclosure. The surfaces can be treated by forming a resistive coating or coatings, by surface

doping, by surface doping and forming a resistive coating or coatings, or by firing to reduce the surface. The resistive coating or coatings can be formed by chemical vapor deposition, sputtering, or evaporation.

Further, the present invention furnishes a light-emitting structure suitable for use in optical devices such as flat-panel CRT displays. The light-emitting structure of the invention contains a main section, a pattern of ridges situated along the main section, and a plurality of light-emissive regions situated along the main section in spaces between the ridges. The light-emissive regions produce light upon being struck by electrons. The ridges, in contrast, are substantially non-emissive of light when hit by electrons. The ridges extend further away from the main section than the light-emissive regions.

Each ridge includes a dark region that encompasses substantially the entire width of that ridge and at least part of its height. The pattern of ridges thereby forms a raised black matrix that improves the contrast of the light-emitting structure. The raised black matrix also enhances the color purity when the light-emissive regions selectively produce light of two or more colors.

In a typical optical device that utilizes the present light-emitting structure, the main section constitutes the first of a pair of plates having internal surfaces that face, and are spaced apart, from each other. The light-emissive regions and the raised ridges are situated along the internal surface of the first plate. The first plate is transparent at least in portions extending along the light-emissive regions. An array of laterally separated sets of electron-emissive elements are situated along the internal surface of the second plate. The electron-emissive elements emit electrons that cause the light-emissive regions to emit light. The optical device contains supporting structure that supports the two plates and keeps them spaced apart from each other.

The support structure preferably includes a group of laterally separated internal supports situated between the ridges and the second plate so as to cross the ridges. The internal supports extend towards areas between the electron-emissive elements. As a result, the internal supports are largely not visible at the exterior surface of the faceplate--i.e., the viewing surface.

The light-emissive regions are typically quite fragile. Because the ridges extend further away from the first plate than the light-emissive regions, the ridges prevent the internal supports from directly exerting force on the light-emissive regions. The combination of internal supports and raised ridges thereby provides a mechanism for maintaining a desired spacing between the two plates along the full active area of the optical device without subjecting the fragile light-emissive regions to potentially damaging mechanical forces produced by the internal supports. This increases device reliability.

The light-emitting structure of the invention can be fabricated according to various techniques. In one group of techniques according to the invention, the pattern of ridges is formed along the main section by a process that involves selectively removing portions of a layer of ridge material provided along the main section. In another group of techniques according to the invention, portions of a body are selectively removed to a specified depth such that the remainder of the body comprises the main section and the pattern of ridges.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective cutaway view of a flat panel display including a thermionic cathode according to an embodiment of the invention.

Figures 2A and 2B are simplified cross-sectional views of a flat panel display according to an embodiment of the invention illustrating the use of spacer walls.

Figure 2A is a cross-sectional view taken along plane 2B-2B of Figure 2B. Figure 2B is a cross-sectional view taken along plane 2A-2A of Figure 2A.

Figure 3 is a perspective cutaway view of a flat panel display including a field emission cathode according to another embodiment of the invention.

Figure 4A is a detailed perspective sectional view of a portion of the flat panel display of Figure 3.

Figures 4B and 4C are plan views of internal parts of the display of Figure 4A as seen respectively from the positions of, and in the directions of, arrows C and D.

Figure 4D is a cross-sectional side view of the full flat-panel CRT display of Figure 4A.

Figure 4E is a magnified cross-sectional structural view of part of the CRT display of Figure 4A centering around the black matrix.

Figure 5 is a detailed view of a portion of Figure 2B illustrating means for aligning spacer walls according to an embodiment of the invention.

Figure 6 is a simplified cross-sectional view, viewed in the same direction as Figure 2A, illustrating a flat panel display including spacer walls and a spacer structure according to another embodiment of the invention.

Figure 7A is a simplified cross-sectional view, viewed in the same direction as Figure 2A, of a portion of a flat panel display according to an embodiment of the invention including a field emission cathode and spacer walls.

Figure 7B is a simplified cross-sectional view, viewed in the same direction as Figure 2A, of a portion of a flat panel display according to another embodiment of the invention including a field emission cathode, spacer walls and an addressing grid.

Figure 7C is a simplified cross-sectional view, viewed in the same direction as Figure 2A, of a portion of a flat panel display according to another embodiment of

the invention including a field emission cathode, a spacer structure and an addressing grid.

Figure 8 is a simplified cross-sectional view, viewed in the same direction as Figure 2A, illustrating the use of spacers according to the invention in a flat panel display having a curved faceplate and backplate.

Figures 9A and 9B are simplified cross-sectional views of a flat panel display according to an embodiment of the invention illustrating a coating formed on surfaces of spacer walls. Figure 9A is a cross-sectional view taken along plane 9B-9B of Figure 9B, and Figure 9B is a cross-sectional view taken along plane 9A-9A of Figure 9A.

Figure 10 is a graph of voltage versus distance from a field emitter in a direction perpendicular to a baseplate on which the field emitter is situated.

Figure 11 is a graph of secondary emission ratio versus voltage illustrating the characteristics of two materials.

Figures 12A through 12D are cross-sectional views illustrating the interface between a spacer wall, metallization and focusing ridges of the backplate according to various embodiments of the invention.

Figures 13A, 13B, 13C, 13D, 13E, 13F, 13G, and 13H are cross-sectional views representing steps in manufacturing a light-emitting black-matrix structure for the display of Figure 4A.

Figures 14A, 14B, 14, 14D, 14E, 14F, 14G, 14H, 14I, and 14J are cross-sectional views representing steps in manufacturing another light-emitting black-matrix structure for the display of Figure 4A.

Figures 15A, 15B, 15C, 15D, 15E, 15F, 15G, 15H, 15I, and 15J are cross-sectional views representing steps in manufacturing a further light-emitting black-matrix structure for the display of Figure 4A.

Figures 16A, 16B, 16C, 16D, 16E, 16F, 16G, 16H, 16I, and 16J are cross-sectional views representing steps in

manufacturing yet another light-emitting black-matrix structure for the display of Figure 4A.

Like reference symbols are employed in the drawings and in the description of the preferred embodiments to represent the same or very similar item or items.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

In the following description, embodiments of the invention are described with respect to a flat cathode ray tube (CRT) display. It is to be understood that the invention is also applicable to other flat panel displays such as plasma displays or vacuum fluorescent displays. Further, the invention is not limited to use with displays, but can be used with other flat panel devices used for other purposes such as optical signal processing, optical addressing for use in controlling other devices such as, for instance, phased array radar devices, or scanning of an image to be reproduced on another medium such as in copiers or printers. Additionally, the invention is applicable to flat panel devices having non-rectangular screen shapes, e.g., circular, and irregular screen shapes such as might be used in a vehicle dashboard or an aircraft control panel.

Herein, a flat panel display is a display in which the faceplate and backplate are substantially parallel, and the thickness of the display is small compared to the thickness of a conventional deflected-beam CRT display, the thickness of the display being measured in a direction substantially perpendicular to the faceplate and backplate. Typically, though not necessarily, the thickness of a flat panel display is less than 2 inches (5.08 cm). Often, the thickness of a flat panel display is substantially less than 2 inches, e.g., 0.25 - 1.0 inches (0.64 - 2.54 cm).

Figure 1 is a perspective cutaway view of flat panel display 100 according to an embodiment of the invention. Flat panel display 100 includes faceplate 102, backplate

103 and layer 105 having peripheral region 105a outside seals 101a, 101b on which electronics 110 are disposed. Faceplate 102, backplate 103, layer 105 and seals 101a, 101b form an enclosure that is held at vacuum pressure (herein, vacuum pressure is defined as any pressure less than atmospheric pressure) of approximately 1 x 10^{-7} torr. Within the enclosure, cathode 109, which is formed on or near backplate 103, is heated to emit electrons toward the phosphor-coated interior surface of faceplate 102 (i.e., anode). Addressing grid 106 is positioned between cathode 109 and faceplate 102. Electronics 110 includes driving circuitry for controlling the voltage of electrodes in holes 111 of addressing grid 106 so that the flow of electrons to faceplate 102 is regulated. Spacers 108 support faceplate 102 against addressing grid 106.

Figure 2A is a simplified cross-sectional view, taken along plane 2B-2B of Figure 2B, of flat panel display 200 according to the invention. Figure 2B is a simplified cross-sectional view, taken along plane 2A-2A of Figure 2A, of flat panel display 200. Faceplate 202, backplate 203, top wall 204a, bottom wall 204c, and side walls 204b, 204d form enclosure 201 that is held at vacuum pressure. The side (interior surface) of faceplate 202 facing into enclosure 201 is coated with phosphor or phosphor patterns. Layer 205 is disposed between faceplate 202 and backplate 203. Addressing grid 206 is formed within enclosure 201 on the portion of layer 205 corresponding to the active region (i.e., projected area of the phosphor coated region of faceplate 202 on a plane parallel to faceplate 202) of faceplate 202. Spacer walls 207 (cathode spacer walls) and 208 (anode spacer walls) are disposed between backplate 203 and addressing grid 206, and faceplate 202 and addressing grid 206, respectively.

Herein, "spacer" is used to describe generally any structure used as an internal support within a flat panel display. In this disclosure, specific embodiments of spacers according to the invention are described as a

"spacer wall" or "spacer walls," or as a "spacer structure." "Spacer" subsumes "spacer wall," "spacer walls," and "spacer structure," as well as any other structure performing the above-described function of a spacer.

A thermionic cathode is located between addressing grid 206 and backplate 203. The thermionic cathode includes cathode wires 209, and directional electrodes 210 formed on cathode spacer walls 207. Though not shown, electrodes could also be formed on backplate 203. Though two directional electrodes 210 are shown formed on each side of each cathode spacer wall 207, it is to be understood that other numbers of directional electrodes 210 could be used. Further, though one cathode wire 209 is shown between each cathode spacer wall 207, it is to be understood that there can be more than one cathode wire 209 between each cathode spacer wall 207.

Each end of each cathode wire 209 is attached to a spring (not shown) by, for instance, welding. The springs are, in turn, attached to backplate 203, addressing grid 206 or cathode spacer walls 207. The springs maintain cathode wires 209 parallel to backplate 203, addressing grid 206 and cathode spacer walls 207 as cathode wires 209 heat and expand during operation of display 200, then cool and contract when display 200 is turned off.

Each cathode wire 209 is heated to release electrons. A voltage is applied to each directional electrode 210 to help shape the electron distribution and electron paths as the electrons move toward addressing grid 206. Voltages applied to electrodes (not shown) formed on the surface of holes 211 formed in addressing grid 206 govern whether the electrons pass through addressing grid 206 to strike the phosphor coated on faceplate 202. Addressing grid 206 may also contain electrodes that direct the electrons to strike a particular phosphor region or regions, and electrodes that focus the electron distribution. As described in more detail below, cathode spacer walls 207

and/or anode spacer walls 208 can be treated to prevent electrostatic charging of spacer walls 207 and/or 208 that can undesirably affect the flow of electrons toward phosphor-coated faceplate 202 and thereby degrade the quality of the image produced by flat panel display 200.

Though a thermionic cathode in which a wire is heated to emit electrons is described above, other types of thermionic cathode can be used. For instance, rather than including a wire, a thermionic cathode (microthermionic cathode) can include dots (the dots can be of any shape) of material formed on backplate 203 which are heated to emit electrons.

Faceplate 202 is made of, for example, glass. Backplate 203 is made of, for example, glass, ceramic, glass-ceramic, silicon or metal. Addressing grid 206 is made of, for example, ceramic or glass-ceramic. Walls 204a, 204b, 204c, 204d are made of, for example, glass, ceramic, glass-ceramic or metal.

Illustratively, the thickness of faceplate 202 is approximately 0.080 inches (2.03 mm), the thickness of addressing grid 206 is approximately 0.020 inches (0.51 mm), and the thickness of backplate 203 is approximately 0.080 inches (2.03 mm).

Phosphor or phosphor patterns are coated on the interior surface of faceplate 202. The region of faceplate 202 in which phosphor is coated is called the active region. (Note: "Active region" has been used elsewhere in this description to denote, in addition to the above-described region of faceplate 202, the projected area of that region of faceplate 202 in any plane parallel to faceplate 202.) Phosphor need not cover the entire active region. The phosphor can be segmented into regions. Phosphor regions can be defined by surrounding them with a black border, called a "black matrix," to improve contrast. In order to avoid a "prison cell effect" on the external viewing surface of faceplate 202, anode spacer walls 208 must be located over the black

matrix within the active region of faceplate 202 so that anode spacer walls 208 are not seen at the viewing surface of flat panel display 200.

In one embodiment of the invention, the black matrix is raised above the phosphor coating on the interior surface of faceplate 202 by photolithographic patterning and etching away of the black matrix material in the areas to be coated with phosphor. Anode spacer walls 208 contact a part of the black matrix. Since the black matrix is raised above the remainder of faceplate 202, even if anode spacer walls 208 slide from their original position on the black matrix, anode spacer walls 208 are held above the phosphor coating by another part of the black matrix so that the phosphor coating is not damaged by contact with anode spacer walls 208, as is evident from the more detailed description of the black matrix below.

In another embodiment of the invention, the surface of the black matrix is approximately level with the phosphor coating on faceplate 202. Again, anode spacer walls 208 contact the black matrix.

Distance 222 between the phosphor-coated interior surface of faceplate 202 and the facing surface of addressing grid 206 depends upon voltage breakdown requirements. In one embodiment, distance 222 is approximately 0.100 inches (2.54 mm). Distance 223 between the interior surface of backplate 203 and the facing surface of addressing grid 206 depends upon the uniformity of the electron flow from the cathode. In one embodiment, distance 223 is approximately 0.250 inches (6.35 mm).

An important aspect of the invention is that, because of the support provided by spacer walls 207 and 208, the above illustrative dimensions are appropriate for flat panel displays having a diagonal (i.e., the diagonal distance between opposite corners of the active region) of any size.

Spacing 225 of cathode spacer walls 207 is determined according to mechanical and electrical constraints. Mechanically, there must be an adequate number of cathode spacer walls 207, positioned properly with respect to addressing grid 206, to properly support backplate 203 against the pressure differential between the vacuum pressure in enclosure 201 and the atmospheric pressure surrounding the exterior of flat panel display 200. Spacing 225 depends upon distance 223 between the interior surface of backplate 203 and the facing surface of addressing grid 206, the material of which cathode spacer walls 207 are made, and the thickness and material of backplate 203.

Electrically, cathode spacer walls 207 must be located so that directional electrodes 210 are an appropriate distance from each cathode wire 209 to achieve the desired distribution and path-shape of electrons emitted from cathode wires 209, and to ensure that the electrons are accelerated adequately toward addressing grid 206. Depending on the particular electrical and geometrical characteristics of flat display 200, either electrical or mechanical constraints may dictate the maximum allowable spacing 225.

In addition to the above constraints, cathode spacer walls 207 must be located so that they do not cover holes 211 formed in addressing grid 206, or adversely intercept or deflect electrons. However, as noted above and described in greater detail below, cathode spacer walls 207 can be treated to minimize or eliminate undesired interception or deflection of electrons.

Spacing 224 of anode spacer walls 208 is also determined according to mechanical and electrical considerations. Mechanically, there must be an adequate number of anode spacer walls 208, positioned properly with respect to addressing grid 206, to properly support faceplate 202 against the pressure differential between the vacuum pressure in enclosure 201 and the atmospheric

pressure surrounding the exterior of flat panel display 200. Similarly to spacing 225, spacing 224 depends upon distance 222 between the interior surface of faceplate 202 and the facing surface of addressing grid 206, the material of which anode spacer walls 208 are made, and the thickness of faceplate 202.

Further, anode spacer walls 208 must be located so that they do not cover holes 211 formed in addressing grid 206, cover phosphor on faceplate 202, or adversely intercept or deflect electrons. Again, however, anode spacer walls 208 can be treated to minimize or eliminate undesired deflection or interception of electrons.

In one embodiment of the invention, for glass faceplate 202 having a thickness of 0.080 inches (2.03 mm), glass-ceramic anode spacer walls 208 having a thickness of 4 mils (0.102 mm), and distance 222 of 0.1 inches (2.54 mm), spacing 224 is approximately 1 inch (2.54 cm). For glass backplate 203 having a thickness of 0.080 inches (2.03 mm), glass-ceramic cathode spacer walls 207 having a thickness of 4 mils (0.102 mm), and distance 223 of 0.25 inches (6.4 mm), spacing 225 is also approximately 1 inch (2.54 cm), taking into consideration only mechanical constraints on spacing 225. However, the maximum spacing 225 of cathode spacer walls 207 may vary from this value because cathode spacer walls 207 can be shaped and because backplate 203 can be made of a material other than glass. Further, as noted above, electrical considerations may dictate a different spacing 225.

Anode spacer walls 208 can be located such that each anode spacer wall 208 is opposite addressing grid 206 from one of cathode spacer walls 207. Anode spacer walls 208 need not be formed opposite each cathode spacer wall 207 if the backplate 203 is sufficiently thick. Further cathode spacer walls 207 need not be formed opposite each anode spacer wall 208.

In the embodiments of the invention discussed so far, cathode spacer walls, e.g., cathode spacer walls 207, have

extended all the way from backplate 203 to addressing grid 206. However, this need not be the case for all cathode spacer walls.

In the above description, spacer walls 207 and 208 follow a straight line path between rows of holes 211 in addressing grid 206 from top wall 204a to bottom wall 204c. In additional embodiments of the invention, spacer walls can follow other than a straight line path through rows of holes 211 in addressing grid 206.

In the above description, spacer walls 207 and 208 extend from close to top wall 204a to close to bottom wall 204c. Generally, spacer walls 207 and 208 can be formed in any manner to provide support so long as they do not adversely affect the electron flow to faceplate 202. For instance, spacer walls 207 and 208 could be formed that extend from one side wall 204b to the other side wall 204d, or spacer walls 207 and 208 could extend diagonally across flat panel display 200. Which of these configurations is chosen will depend on the characteristics of the cathode.

Spacer walls 207 and 208 must have a sufficiently small thickness so that spacer walls 207 and 208 do not overlap and block holes 211 in addressing grid 206. In one embodiment of the invention, holes 211 are approximately 5 mils (0.127 mm) in diameter and have a center-to-center distance, measured between holes 211 in the same row or column, of 12.5 mils (0.318 mm). Spacer walls 207 and 208 have a thickness of approximately 4 mils (0.102 mm).

Generally, spacer walls and spacer structures in embodiments of the invention described above and below are made of a thin material which is readily workable in an untreated state and becomes stiff and strong after a prescribed treatment. The material must also be compatible with use in a vacuum environment. Further, the spacer walls and spacer structures are made of a material having a coefficient of thermal expansion that closely

matches the coefficients of thermal expansion of the faceplate, backplate and addressing grid (if present). Matching the coefficients of thermal expansion means that the spacer walls, addressing grid, faceplate and backplate expand and contract approximately the same amount during heating and cooling that occurs when the flat panel display is assembled or operated. Consequently, proper alignment is maintained among the spacer walls, addressing grid, faceplate and backplate. Possible consequences of not matching coefficients of thermal expansion are: damage to the phosphor resulting from movement of anode spacer walls or spacer structure relative to the faceplate, stresses within the flat panel display that might cause parts of the flat panel display to fail (including failure of display vacuum integrity), or failure of the anode or cathode spacer walls. Another important aspect of the invention is that the spacer walls and spacer structures can be made of the same material used to form the addressing grid (if present).

In one embodiment, spacer walls 207 and 208 are made of a ceramic or glass-ceramic material. In another embodiment, spacer walls 207 and 208 are formed from ceramic tape. Hereafter, in description of embodiments of the invention, ceramic or glass-ceramic tapes and slurries are the materials used for the spacer walls or spacer structures.

Other materials, such as ceramic reinforced glass, devitrified glass, amorphous glass in a flexible matrix, metal with electrically insulative coating, or high-temperature vacuum-compatible polyimides, could be used. Broadly speaking, the requirements of the material for spacers according to the invention are that (a) it be producible in thin layers, (b) the layers be flexible in the unfired state, (c) holes can be put in a layer or several layers together in the unfired state, (d) the holes can be filled with conductors where desired, (e) conductive traces can be put accurately on the surfaces of

the unfired layers, (f) the layers can be laminated, in that they are bonded together at least on a final firing, (g) the fired structure have a coefficient of thermal expansion that can be substantially matched to that of a face plate and a back plate which are made of materials such as float glass, (h) the fired, laminated structure be rigid and strong, (i) the fired structure be vacuum compatible, (j) the fired structure not contain materials which will poison the cathode of the CRT, and (k) all materials and fabrication be possible at practical cost.

In this description and in the claims which follow, the term "ceramic" is often used, in the context of ceramic tape or ceramic layer or ceramic sheet. The term is intended to refer to any of a known family of glass-ceramic tapes, devitrifying glass tapes, ceramic glass tapes, ceramic tapes or other tapes which have plastic binders and ceramic or glass particles and which are flexible and workable in the unfired state, curable to a hard and rigid layer on firing, as well as other materials equivalent thereto, which are initially flexible and may be processed to a final hard and rigid state.

Ceramic tape is formed from a mixture of ceramic particles, amorphous glass particles, binders and plasticizers. Initially, the mixture is a slurry which can be molded instead of formed into ceramic tape. Ceramic tape can be formed from the slurry and, in an unfired state, is a deformable material which can easily be cut and formed as desired. Ceramic tape may be made in thin sheets, e.g., approximately 0.3 to 10 mils. Examples of ceramic tape that can be used with the invention are the tapes available from Coors Electronic Package Co. of Chattanooga, Tennessee as Catalog Nos. CC-92771/777 and CC-LT20, or tapes that are the substantial equivalent of the Coors ceramic tape.

Another example of a low temperature glass-ceramic material which can be used for the purposes of this invention is du Pont's Green Tape (trademark of du Pont).

Green Tape is available in very thin sheets (e.g. about 3 mils to 10 mils) has a relatively low firing temperature, about 900°C to 1000°C, and includes plasticizers in the unfired state which provide excellent workability. The Green Tape product is a mixture of ceramic particles and amorphous glass, also in particulate form, with binders and plasticizers. See U.S. Patent Nos. 4,820,661, 4,867,935, and 4,948,759.

Unfired ceramic tape can readily be formed in the ways to be described below to yield spacer walls and spacer structures according to the invention. After forming, the ceramic tape is fired. The firing occurs in two stages: a first stage in which the tape is heated to a temperature of approximately 350°C to burn out the binders and plasticizers from the tape, and a second stage in which the tape is heated to a temperature (between 800°C and 2000°C, depending on the composition of the ceramic) at which the ceramic particles sinter together to form a strong, dense structure.

Spacer walls 207 and 208 of Figures 2A and 2B are formed and assembled into flat panel display 200 as follows. Strips, having a length and width chosen according to the particular requirements of flat panel display 200, as explained in more detail above, are cut from a sheet of unfired ceramic tape. An advantage of using an unfired ceramic or glass-ceramic is that the strips can be easily fabricated by slitting or die-cutting. The strips are then fired, as described above. The fired strips (spacer walls 207 and 208) are placed at appropriate pre-determined locations with respect to addressing grid 206, faceplate 202 and backplate 203, and attached to addressing grid 206 by, for instance, gluing or glass fritting. During assembly, spacer walls 207 and 208 are held in place so that they are properly aligned with respect to faceplate 202, backplate 203 and addressing grid 206. Proper alignment of spacer walls 207

and 208 can be achieved using, for example, the approach described in more detail below with respect to Figure 5.

The strips for spacer walls 207 and 208 can also be fabricated by first making and firing sheets of ceramic or glass-ceramic. The fired sheets can then be coated (as explained in more detail below) and cut into strips that form spacer walls 207 and 208. Alternatively, the fired sheets can be cut into strips and then coated.

Figure 3 is a perspective cutaway view of flat panel display 300 according to another embodiment of the invention. Flat panel display 300 includes faceplate 302, backplate 303 and side walls 304 which together form sealed enclosure 301 that is held at vacuum pressure, e.g., approximately 1 x 10^{-7} torr or less. Spacer walls 308 support faceplate 302 against backplate 303.

Field emitter cathode 305 is formed on a surface of backplate 303 within enclosure 301. As explained in more detail below, row and column electrodes (not shown) control the emission of electrons from a cathodic emission element (not shown). The electrons are accelerated toward the phosphor-coated interior surface of faceplate 302 (i.e., anode), as also explained in more detail below. Integrated circuit chips 310 include driving circuitry for controlling the voltage of the row and column electrodes so that the flow of electrons to faceplate 302 is regulated. Electrically conductive traces (not shown) are used to electrically connect circuitry on chips 310 to the row and column electrodes.

Figure 4A illustrates part of a flat-panel color CRT display that employs an area field-emission cathode in combination with a raised black matrix. The CRT display in Figure 4A contains transparent electrically insulating flat faceplate 302 and electrically insulating flat backplate 303. The internal surfaces of plates 302 and 303 face each other and are typically 0.01 - 2.5 mm apart. Faceplate 302 consists of glass typically having a

thickness of 1 mm. Backplate 303 consists of glass, ceramic, or silicon typically having a thickness of 1 mm.

A group of laterally separated electrically insulating spacer walls 308 are situated between plates 302 and 303. Spacer walls 308 extend parallel to one another at a uniform spacing. Walls 308 extend perpendicular to plates 302 and 303. Each wall 308 consists of ceramic typically having a thickness of 80 - 90 μm. The center-to-center spacing of walls 308 is typically 8 - 25 mm. As discussed further below, walls 308 constitute internal supports for maintaining the spacing between plates 302 and 303 at a substantially uniform value across the entire active area of the display.

Patterned area field-emission cathode structure 305 is situated between backplate 303 and spacer walls 308. Figure 4B depicts the layout of field-emission cathode structure 305 as viewed in the direction, and from the positions, represented by arrows C in Figure 4A. Cathode structure 305 consists of a large group of electron-emissive elements 309, a patterned metallic emitter electrode (sometimes referred to as base electrode) divided into a group of substantially identical straight lines 310, a metallic gate electrode divided into a group of substantially identical straight lines 311, and an electrically insulating layer 312.

Emitter-electrode lines 310 are situated on the interior surface of backplate 303 and extend parallel to one another at a uniform spacing. The center-to-center spacing of emitter lines 310 is typically 315 - 320 μm. Lines 310 are typically formed of molybdenum or chromium having a thickness of 0.5 μm. Each line 310 typically has a width of 100 μm. Insulating layer 312 lies on lines 310 and on laterally adjoining portions of backplate 303. Insulating layer 312 typically consists of silicon dioxide having a thickness of 1 μm.

Gate-electrode lines 311 are situated on insulating layer 312 and extend parallel to one another at a uniform spacing. The center-to-center spacing of gate lines 311 is typically 105 - 110 μm. Gate lines 311 also extend perpendicular to emitter lines 310. Gate lines 311 are typically formed with a titanium-molybdenum composite having a thickness of 0.02 - 0.5 μm. Each line 311 typically has a width of 30 μm.

Electron-emissive elements 309 are distributed above the interior surface of backplate 303 in an array of laterally separated multi-element sets. In particular, each set of electron-emissive elements 309 is located above the interior surface of backplate 303 in part or all of the projected area where one of gate lines 311 crosses one of emitter lines 310. Spacer walls 308 extend towards areas between the sets of electron-emissive elements 309 and also between emitter lines 310.

Each electron-emissive element 309 is a field emitter that extends through an aperture (not shown) in insulating layer 310 to contact an underlying one of emitter lines 310. The top (or upper end) of each field emitter 309 is exposed through a corresponding opening (not shown) in an overlying one of gate lines 311.

Field emitters 309 can have various shapes such as needle-like filaments or cones. The shapes of field emitters 309 is not particularly material here as long as they have good electron-emission characteristics. Emitters 309 can be manufactured according to various processes, including those described in Macaulay et al, commonly owned U.S. patent application Ser. No. 08/118,490, "Structure and Fabrication of Filamentary Field-Emission Device, Including Self-Aligned Gate," filed 8 September 1993, and Spindt et al, commonly owned U.S. patent application Ser. No. 08/158,102, "Field-Emitter Fabrication Using Charged-Particle Tracks, and Associated Field-Emission Devices," filed 24 November 1993. The

contents of Ser. Nos. 08/118,490 and 08/158,102 are incorporated by reference herein.

A light-emitting structure which contains a black matrix is situated between faceplate 302 and spacer walls 308. The light-emitting structure consists of a group of light-emissive regions 313, a pattern of substantially identical dark ridges 314 that reflect substantially no light, and light-reflective layer 315. Figure 4C depicts the layout of the light-emitting structure as viewed in the direction, and from the positions, represented by arrows D in Figure 4A.

Light-emissive regions 313 and dark ridges 314 are both situated on the interior surface of faceplate 302. Light-emissive regions 313 are located in spaces between dark ridges 314 (or vice versa). When regions 313 and ridges 314 are struck by electrons emitted from electron-emissive elements 309, light-emissive regions 313 produce light of various colors. Dark ridges 314 are substantially non-emissive of light relative to light-emissive regions 313 and thereby form a black matrix for regions 313.

More specifically, light-emissive regions 313 consist of phosphors configured in straight equal-width stripes extending parallel to one another at a uniform spacing in the same direction as gate lines 311. Each phosphor stripe 313 typically has a width of 80 μm. The thickness (or height) of phosphor stripes 313 is 1 - 30 μm, typically 25 μm.

Phosphor stripes 313 are divided into a plurality of substantially identical stripes 313r that emit red (R) light, a like plurality of substantially identical stripes 313g that emit green (G) light, and another like plurality of substantially identical stripes 313b (B) that emit blue light. Phosphor stripes 313r, 313g, and 313b are repeated at every third stripe 313 as indicated in Figure 4A. Each phosphor stripe 313 is situated across from a corresponding one of gate lines 311. Consequently, the

center-to-center spacing of stripes 313 is the same as that of gate lines 311.

Dark ridges 314 similarly extend parallel to one another at a uniform spacing in the same direction as gate lines 311. The center-to-center spacing of ridges 314 is likewise the same as that of lines 311. The ratio of the average height of each dark ridge 314 to its average width is in the range of 0.5 - 3, typically 2. The average width of ridges 314 is 10 - 50 μm, typically 25 μm. The average height of ridges 314 is 20 - 60 μm, typically 50 μm.

The average height of dark ridges 314 exceeds the thickness (or height) of phosphor stripes 313 by at least 2 μm. In the typical case described above, ridges 314 extend 25 μm above stripes 313. Accordingly, ridges 314 extend further away from faceplate 302 than stripes 313.

Each ridge 314 contains a dark (essentially black), non-reflective region that occupies the entire width of that ridge 314 and at least part of its height. Figure 4A depicts an example in which these dark non-reflective regions encompass the full height of ridges 314. The later drawings illustrate examples in which the dark non-reflective regions occupy only parts of the ridge height.

The choice of materials for dark ridges 314 is wide. Ridges 314 can be formed with metals such as nickel, chrome, niobium, gold, and nickel-iron alloys. Ridges 314 can also be formed with electrical insulators such as glass, solder glass (or frit), ceramic, and glass-ceramic, with semiconductors such as silicon, and with materials such as silicon carbie. Combinations of these materials can also be utilized in ridges 314.

When ridges 314 consist of metal, they become sufficiently soft at a temperature in the range of 300-600°C as to allow objects, such as spacer walls 308, to be pushed slightly into them. When ridges 314 are formed with solder glass, they so soften at a temperature in the ranges of 300-500°C. When the ridge material is glass,

ridges 314 soften at a temperature in the range of 500-700°C.

Light-reflective layer 315 is situated on phosphor stripes 313 and dark ridges 314 as shown in Figure 4B. The thickness of layer 315 is sufficiently small, typically 50 - 100 nm, that nearly all of the impinging electrons from electron-emissive elements 309 pass through layer 315 with little energy loss.

The surface portions of light-reflective layer 315 adjoining phosphor stripes 313 are quite smooth. Layer 315 consists of a metal, preferably aluminum. Part of the light emitted by stripes 313 is thus reflected by layer 315 through faceplate 302. That is, layer 315 is basically a mirror. Layer 315 also acts as the final anode for the display. Because stripes 313 contact layer 315, the anode voltage is impressed on stripes 313.

Spacer walls 308 contact light-reflective layer 315 on the anode side of the display. Because dark ridges 314 extend further toward backplate 303 than phosphor stripes 313, walls 308 specifically contact portions of layer 315 along the tops (or bottoms in the orientation shown in Figure 4A) of ridges 314. The extra height of ridges 314 prevents walls 308 from contacting light-reflective layer 315 along phosphor stripes 313.

On the cathode side of the display, spacer walls 308 are shown as contacting gate lines 311 in Figure 4A. Alternatively, walls 308 may contact focusing ridges that extend above lines 311 as described in Spindt et al, U.S. patent application Ser. No. _____, "Field Emitter with Focusing Ridges Situated to Sides of Gate" (Attorney Docket No. M-2691), filed _____ 1994, the contents of which are incorporated by reference herein. Walls 308 can be manufactured in a conventional manner or as described herein.

The air pressure external to the display is normally atmospheric--i.e., in the vicinity of 760 torr. The internal pressure of the display is normally set at a

value below 10^{-7} torr. Since this is much less than the normal external pressure, high differential pressure forces are usually exerted on plates 302 and 303. Spacer walls 308 resist these pressure forces.

Phosphor stripes 313 can be damaged easily if mechanically contacted. Because the extra height of dark ridges 314 creates spaces between walls 308 and the portions of light-reflective layer 315 along stripes 313, walls 308 do not exert their resistance forces directly on stripes 313. The amount of damage that stripes 313 could otherwise incur as a result of these resistive forces is greatly reduced.

The display is subdivided into an array of rows and columns of picture elements ("pixels"). The boundaries of a typical pixel 316 are indicated by lines with arrowheads in Figure 4A and by dotted lines in Figures 4B and 4C. Each emitter line 310 is a row electrode for one of the rows of pixels. For ease of illustration, only one pixel row is indicated in Figures 4A, 4B, and 4C as being situated between a pair of adjacent spacer walls 308 (with a slight, but inconsequential, overlap along the sides of the pixel row). However, two or more pixel rows, typically 24 - 100 pixel rows, are normally located between each pair of adjacent walls 308.

Each column of pixels has three gate lines 311: (a) one for red, (b) a second for green, and (c) the third for blue. Likewise, each pixel column includes one of each of phosphor stripes 313r, 313g, and 313b. Each pixel column utilizes four of dark ridges 314. Two of ridges 314 are internal to the pixel column. The remaining two are shared with pixel(s) in the adjoining column(s).

Light-reflective layer 315 and, consequently, phosphor stripes 313 are maintained at a positive voltage of 1,500 - 10,000 volts relative to the emitter-electrode voltage. When one of the sets of electron-emissive elements 309 is suitably excited by appropriately adjusting the voltages of emitter lines 310 and gate lines

311, elements 309 in that set emit electrons which are accelerated towards a target portion of the phosphors in corresponding stripe 313. Figure 4A illustrates trajectories 317 followed by one such group of electrons. Upon reaching the target phosphors in corresponding stripe 313, the emitted electrons cause these phosphors to emit light represented by items 318 in Figure 4A.

Some of the electrons invariably strike parts of the light-emitting structure other than the target phosphors. The tolerance in striking off-target points is less in the row direction (i.e., along the rows) than in the column direction (i.e., along the columns) because each pixel includes phosphors from three different stripes 313. The black matrix formed by dark ridges 314 compensates for off-target hits in the row direction to provide sharp contrast as well as high color purity.

Figure 4D depicts a cross section of the full CRT of Figure 4A. An electrically insulating outer wall 304 extends between plates 302 and 303 outside the active device area to create a sealed enclosure 301. Outer wall 304, which can be formed by four individual walls arranged in a square or rectangle, typically consists of glass or ceramic having a thickness of 2 - 3 mm. As indicated in Figure 4D, spacer walls 308 typically extend close to outer wall 304. Spacer walls 308 could, however, contact outer wall 304.

Back plate 303 extends laterally beyond faceplate 302. Electronic circuitry (not shown) such as leads for accessing emitter lines 310 and gate lines 311 is mounted on the interior surface of back plate 303 outside outer wall 304. Light-reflective layer 315 extends through the perimeter seal to a contact pad 319 to which the anode/phosphor voltage is applied.

Figure 4E presents an enlarged view of part of the light-emitting black-matrix structure in the CRT display of Figure 4A. For exemplary purposes, each dark ridge 314 in Figure 4E is illustrated as consisting of a dark main

portion 314a and a light further portion 314b. Dark portion 314a, which is situated between faceplate 302 and light portion 314b, extends across the entire width of ridge 314 in Figure 4E. Light portion 314b is formed with material that can be transparent. Figure 4E also shows that the surface portions of aluminum light-reflective layer 315 along the interface between phosphors 313 and layer 315 is smooth even though the surface of phosphors 313 along the phosphor/aluminum interface is rough.

Figure 5 is a detailed view of a portion of Figure 2B illustrating means for aligning spacer walls 207 or 208 according to an embodiment of the invention. Notch 504 is formed, by, for instance, cutting, in a direction perpendicular to the plane of Figure 5, in top wall 204a of flat panel display 200 at a location corresponding to the location of anode spacer wall 208.

During assembly of flat panel display 200, end 208a of anode spacer wall 208 is inserted into notch 504 and end 208b (Figure 2B) is inserted into a similar notch formed in bottom wall 204c so that anode spacer wall 208 is held in place. Width 504a of notch 504 is made slightly larger than the thickness of anode spacer wall 208 so that anode spacer wall 208 is held in place in the direction parallel to top wall 204a in the plane of Figure 5. In one embodiment, the thickness of anode spacer wall 208 is 4 mils (0.102 mm), and width 504a is approximately 4.5 mils (0.0114 mm).

Depth 504b of notch 504 is made sufficiently large so that, given dimensioning tolerances, anode spacer wall 208 will fit into, and not slip out of, notch 504. Depth 504b of notch 504 is, illustratively, approximately 10 mils (0.25 mm). Anode spacer wall 208 is made sufficiently long so that if end 208a begins to move out of notch 504, end 208b (Figure 2B) contacts a corresponding notch formed in bottom wall 204c before end 208a can move completely out of notch 504. Consequently, anode spacer wall 208 is held in place in the direction perpendicular to top

wall 204a. If, for instance, depth 504b is 10 mils (0.25 mm), anode spacer wall 208 is made slightly less than 10 mils (0.25 mm) longer than the distance 221 (Figure 2A) between top wall 204a and bottom wall 204c of flat panel display 200.

In an alternative embodiment, rather than cutting notches in the top wall 204a and bottom wall 204c, respectively, as described above, a notch is formed in addressing grid 206 into which anode spacer wall 208 fits. During assembly of flat panel display 200, anode spacer wall 208 is inserted into the notch in addressing grid 206. The width of the notch is made slightly larger than the thickness of anode spacer wall 208. In one embodiment, the width of the notch is approximately 4.5 mils (0.0114 mm). The depth of the notch is, illustratively, approximately 1 - 2 mils (0.025 - 0.051 mm). Anode spacer 208 is made slightly less than 1 - 2 mils (0.025 - 0.051 mm) wider than distance 222 between faceplate 202 and addressing grid 206.

In another embodiment, notches are cut, as described above, in each of top wall 204a, bottom wall 204c and addressing grid 206.

In a further embodiment in which a field emission cathode is used, notches of appropriate size are cut into baseplate 203 into which spacer walls 207 fit.

Though the above description with respect to Figure 5 is made with respect to end 208a of anode spacer walls 208, it is to be understood that end 208b (Figure 2B) is held in place during formation of flat panel display 200 using similar means. Further, cathode spacer walls 207 can be held in place during formation of flat panel display 200 using means similar to that described for anode spacer walls 208. Additionally, if spacer walls 207 and 208 extend between side walls 204b and 204d, notches are cut in side walls 204b and 204d, as described above. Finally, though formation of notches for aligning spacer walls according to the invention is described above with

respect to flat panel display 200 including a thermionic cathode, it is to be understood that such notches can also be formed in a flat panel display, e.g., flat panel display 300 (Figure 3), including a field emitter cathode.

Figure 6 is a simplified cross-sectional view, viewed in the same direction as Figure 2A, illustrating flat panel display 600 including cathode spacer walls 607 and anode spacer structure 608 according to another embodiment of the invention. Faceplate 602, backplate 603, a top wall (not shown), a bottom wall (not shown), and side walls 604a, 604b form enclosure 601 which is held at vacuum pressure, e.g., approximately 1 x 10^{-7} torr. The interior side of faceplate 602 is coated with phosphor. Layer 605 is formed between faceplate 602 and backplate 603 within enclosure 601 and extends through a sealed area of the top wall, bottom wall and side walls 604a, 604b to the outside of enclosure 601. Addressing grid 606 is formed on the portion of layer 605 corresponding to the active region of faceplate 602. Cathode spacer walls 607 and anode spacer structure 608 (referred to as a "grid-to-grid spacer structure") are disposed between backplate 603 and addressing grid 606, and faceplate 602 and addressing grid 606, respectively.

A thermionic cathode is located between addressing grid 606 and backplate 603. The thermionic cathode includes cathode wires 609, backing electrodes 612 and electron steering grids 613. Cathode wire 609 is heated to release electrons. A voltage may be applied to backing electrode 612 to help direct the electrons toward addressing grid 606. Electron steering grid 613 may be used to help extract electrons from cathode wire 609 and distribute the flow of electrons evenly between each cathode spacer wall 607. Voltages applied to electrodes (not shown) formed on the surface of holes 611 formed in addressing grid 606 govern whether the electrons pass through addressing grid 606. Electrons that pass through addressing grid 606 continue through holes 614 in anode

spacer structure 608 to strike the phosphor coated on faceplate 602.

In Figure 6, one cathode wire 609 is shown between each cathode spacer wall 607. It is to be understood that there can be more than one cathode wire 609 between each cathode spacer wall 607.

Cathode spacer walls 607 are formed and assembled into flat panel display 600 as described above for cathode spacer walls 207 of Figures 2A and 2B. Anode spacer structure 608 is formed as follows. Several layers of unfired ceramic or glass-ceramic material, e.g., ceramic tape, having the same length and width are laminated together by being held together under pressure and heated to a temperature of approximately 70 °C. Holes 614 are formed through the multilayered laminate structure at locations corresponding to holes 611 in addressing grid 606. Holes 614 can be formed in each layer before lamination, in several layers laminated together, or at one time through all of the layers in the multilayer laminate structure. The multilayer laminate structure (anode spacer structure 608) is then fired, either alone or with addressing grid 606, in a two-stage firing, as described above with respect to formation of spacer walls according to the invention, to remove binders and impart stiffness and strength.

Holes 614 can be formed by a number of methods, including, but not limited to, laser drilling, fluid pressure drilling, etching, molding, or mechanical drilling or punching. Addressing grid 606 can be used as a mask for forming holes 614 in anode spacer structure 608 if holes 614 are formed by drilling or etching.

Holes 614 of anode spacer structure 608 can be formed coaxially with holes 611 of addressing grid 606 or holes 614 can be made larger than holes 611 so that each hole 614 encompasses more than one hole 611. In one embodiment, holes 614 are formed coaxially with holes 611 such that the diameter of holes 614 is larger than the

diameter of holes 611. The larger diameter holes 614 allow more room for error in aligning holes 611 and 614.

In alternative embodiments, the diameter of holes 614 remains constant throughout the length of holes 614 or the diameter of holes 614 gradually increases along the length of holes 614 in a direction toward faceplate 602. In the latter embodiment, holes 614 may overlap each other adjacent faceplate 602. However, some portion of anode spacer structure 608 must remain between holes 614 to contact faceplate 602 to provide support between addressing grid 606 and faceplate 602.

Cathode spacer walls 607 and anode spacer structure 608 can be made of the same material as addressing grid 606. Using the same material, having the same coefficient of thermal expansion, for cathode spacer walls 607, anode spacer structure 608 and addressing grid 606 means that when cathode spacer walls 607, anode spacer structure 608 and addressing grid 606 are heated during assembly or operation of flat panel display 600, cathode spacer walls 607, anode spacer structure 608 and addressing grid 606 will each expand and contract the same amount so that registry of holes 611 and 614 is maintained and cathode spacer walls 607 do not overlap holes 611. Consequently, cathode spacer walls 607, anode spacer structure 608 and addressing grid 606 are more easily formed, since no compensation for different thermal expansion coefficients must be made in order to maintain registry between holes 611 and 614, and alignment between cathode spacer walls 607 and addressing grid 606 when assembling cathode spacer walls 607, anode spacer structure 608 and addressing grid 606.

In an alternative embodiment, anode spacer structure 608 and addressing grid 606 can be formed at the same time by laminating together all of the layers used to form anode spacer structure 608 and addressing grid 606, then firing the combined structure as described above. Additionally, if anode spacer structure 608 and addressing

grid 606 are made of the same material, holes 614 and 611 in anode spacer structure 608 and addressing grid 606, respectively, can be formed at the same time by laminating together all of the layers used to form anode spacer structure 608 and addressing grid 606, then forming holes 614 and 611 using one of the methods described above before firing the combined structure.

If desired, metallization can be formed on some or all of the layers of anode spacer structure 608. Such metallization could be, for instance, electrodes formed on the walls of holes 614 that are used for focusing the electrons or for fixing the voltage at certain locations within holes 614 of spacer structure 608 as the electrons move toward faceplate 602.

Though, in the above description, holes having a circular cross-sectional shape are formed through anode spacer structure 608, holes having other cross-sectional shapes could be formed, e.g., "racetrack," oval, rectangular, diamond, etc.

Figure 7A is a simplified cross-sectional view, viewed in the same direction as Figure 2A, of a portion of flat panel display 700 according to an embodiment of the invention, illustrating the use of anode spacer walls 708 in flat panel display 700 including a field emitter cathode (FEC) structure. A particular type of FEC structure is shown in Figure 7A and a similar FEC structure is shown in Figures 7B and 7C below.

The FEC structure includes row electrodes 710 formed on electrically insulative backplate 703. Insulator 712 (made of an electrically insulative material) is formed on backplate 703 to cover row electrodes 710. Holes 712a are formed through insulator 712 to row electrodes 710. Emitters 709 are formed on row electrodes 710 within holes 712a. Emitters 709 are cone-shaped and tip 709a of emitter 709 extends just above the level of insulator 712. It is to be understood that other types of emitters could be used. Column electrodes 711 are formed on insulator

712 around holes 712a such that column electrodes 711 extend partially over holes 712a to a predetermined distance from emitter tips 709a.

An open space separates column electrodes 711 and emitter tips 709a from faceplate 702. The open space between the FEC structure and faceplate 702 is sealed and held at vacuum pressure, e.g., approximately 10^{-7} torr or less. Phosphor 713 is formed on the surface of faceplate 702 facing the FEC structure. Emitters 709 are excited to release electrons 714 which are accelerated across the open space to strike the phosphor 713 on faceplate 702. When phosphor 713 is struck by electrons 714, phosphor 713 emits light which can be seen through faceplate 702.

Anode spacer walls 708 extend from the column electrodes 711 to faceplate 702 to support faceplate 702 against the force arising from the differential pressure between the vacuum pressure within flat panel display 700 and the ambient atmospheric pressure outside of flat panel display 700. Anode spacer walls 708 are formed in the same manner as anode spacer walls 208 used with a thermionic cathode, as described above with respect to Figures 2A and 2B. Any of the embodiments of anode spacer walls used above with thermionic cathodes can be used with flat panel display 700. Alternatively, an anode spacer structure such as anode spacer structure 608 described above (Figure 6) can be used with flat panel display 700.

Figure 7B is a simplified cross-sectional view, viewed in the same direction as Figure 2A, of a portion of flat panel display 750 according to another embodiment of the invention, illustrating the use of anode spacer walls 758 in flat panel display 750 including a FEC structure and addressing grid 756. The construction and use of an addressing grid with a FEC is described in detail in commonly owned, co-pending U.S. Patent Application Serial No. 08/012,297, entitled "Grid Addressed Field Emission Cathode," by Robert M. Duboc, Jr. and Paul A. Lovoi, filed

on February 1, 1993, the disclosure of which is herein incorporated by reference.

Flat panel display 750 includes faceplate 752 and backplate 753 which, together with side walls (not shown), form a sealed enclosure that is held at vacuum pressure. An insulating layer 762 is formed on an interior surface of backplate 753. Emitters 759 are formed on backplate 753 in holes 762a formed in insulating layer 762. Addressing grid 756 is disposed on insulating layer 762. Holes 756a are formed through addressing grid 756 such that holes 756a are coaxial with holes 762a of insulating layer 762. Electrical conductors 756b are formed in addressing grid 756 and extend to holes 756a. Emitters 759 release electrons 764 which are accelerated through holes 762a and 756a by application of appropriate voltages to electrical conductors 756b to hit phosphor regions 763 formed on an interior surface of faceplate 752.

Anode spacer walls 758 support faceplate 752 against the force arising from the differential pressure between the internal vacuum pressure and the external atmospheric pressure. Anode spacer walls 758 are located so that anode spacer walls 758 do not interfere with the flow of electrons 764. Anode spacer walls 758 are formed as described above. Any of the embodiments of anode spacer walls described above can be used.

Rather than anode spacer walls, an anode spacer structure can be used. Figure 7C is a simplified cross-sectional view, viewed in the same direction as Figure 2A, of a portion of flat panel display 770 according to another embodiment of the invention, illustrating the use of anode spacer structure 778 in flat panel display 770 including a field emitter cathode (FEC) structure and addressing grid 756. Flat panel display 770 is similar to flat panel display 750 except that spacer structure 778 is used instead of spacer walls 758. Spacer structure 778 is formed in the same manner as the spacer structures, e.g., spacer structure 608 (Figure 6), described above. Any of

the embodiments or variations of a spacer structure described above can be used.

In embodiments of the invention described above including a thermionic cathode, cathode spacer walls are used to support the backplate against the addressing grid. As previously noted, a microthermionic cathode in which electrodes are emitted from dots of material formed on the backplate can be used instead of a thermionic cathode in which electrons are emitted from a cathode wire. A microthermionic cathode is structured in a way that is similar to the field emitter cathode structures described above. Consequently, it is possible to use a cathode spacer structure, similar to the anode spacer structure described above, between the backplate and the addressing grid to provide internal support between the backplate and addressing grid of the flat panel display. Such a cathode spacer structure can be used in flat panel displays including either an anode spacer structure or anode spacer walls.

Figure 8 is a simplified cross-sectional view, viewed in the same direction as Figure 2A, illustrating the use of spacer walls 807 and 808 in a curved flat panel display 800 according to the invention. Flat panel display 800 is similar to flat panel display 200, except that faceplate 802, backplate 803 and layer 805 (including addressing grid 806) are each curved so that flat panel display 800 is concave as seen by a viewer. Flat panel display 800 could also be made convex as seen by a viewer.

In each of the above-described embodiments, the spacers must not interfere with the trajectory of the electrons passing between the cathode and the phosphor coating on the faceplate. Thus, the walls of the spacers must be sufficiently electrically conductive so that the spacers do not charge up and attract or repel the electrons to a degree that unacceptably distorts the paths of the electrons. Additionally, the spacers must be sufficiently electrically insulative so that there is no

large current flow from the high voltage phosphor resulting in large power losses. Spacers formed from electrically insulative material and coated with a thin electrically conductive material are preferred.

Figure 9A is a simplified cross-sectional view of a portion of flat panel display 900 including coating 904 formed on spacer walls 908 according to an embodiment of the invention, taken along plane 9B-9B of Figure 9B. Figure 9B is a simplified cross-sectional view of a portion of flat panel display 900, taken along plane 9A-9A of Figure 9A. Flat panel display 900 includes faceplate 902, backplate 903 and side walls (not shown) which together form sealed enclosure 901 that is held at vacuum pressure, e.g., approximately 1 x 10^{-7} torr or less.

Focusing ribs (or ridges) 912 are situated above the interior surface of backplate 903 and perpendicular to the plane of Figure 9A. The use and formation of focusing ribs in a flat panel display is described in more detail in commonly owned, co-filed U.S. Patent Application Serial No. _____, entitled "Field Emitter with Focusing Ridges Situated to Sides of Gate" (Attorney Docket No. M-2691), by Christopher J. Spindt et al., the pertinent disclosure of which is herein incorporated by reference. In the trough formed between each pair of focusing ribs 912, field emitters 909 are formed on an interior surface of backplate 903. Field emitters 909 are formed in groups of approximately 1000.

A matrix of dark ridges 911 is situated within enclosure 901 on faceplate 902, as described in more detail above with respect to Figures 4A - 4E. Phosphor 913 is formed to partially fill each trough between ridges 911. Anode 914, which is a thin electrically conductive material such as aluminum, is formed on phosphor 913.

Spacer walls 908 support faceplate 902 against backplate 903. The surfaces of each spacer wall 908 intermediate the opposing ends are coated with resistive coating 904 or are surface doped, as described in more

detail below. Resistive coating 904 prevents or minimizes charge build-up on spacer wall 908 that can distort the flow of electrons 915.

One end of each spacer wall 908 contacts a plurality of ridges 911 and is coated with edge metallization 905. An opposite end of each spacer wall 908 contacts a plurality of focusing ribs 912 and is coated with edge metallization 906. Edge metallization 905 and 906 can be made of, for instance, aluminum or nickel. Edge metallization 905 and 906 provide good electrical contact between coating 904 and faceplate 902 or focusing ribs 912, respectively, so that the voltage at the ends of spacer walls 904 is well-defined and a uniform ohmic contact is formed. The interface between spacer wall 908, coating 904 and edge metallization 905 can take on a number of configurations, as described in more detail below. Electrodes 917 are formed on the coated (or doped) surfaces of each spacer wall 908, and are used to "segment" the voltage rise from emitters 909 to anode 914.

In another embodiment of the invention, spacer walls 908 are formed without electrodes 917.

Each group of field emitters 909 emit electrons 915 toward the interior surface of faceplate 902. Circuitry (not shown) is formed as part of flat panel display 900, e.g., on integrated circuit chips that can be attached to, for instance, an exterior surface of backplate 903, and used to control the voltage of electrodes 917. Typically, the voltage of each of electrodes 917 is set so that the voltage increases linearly from the voltage level at field emitters 909 to the higher voltage at anode 914. Thus, electrons 915 are accelerated toward faceplate 902 to strike phosphor 913 and cause light to emanate from flat panel display 900.

For optimum focusing, the desired equipotential lines, in the plane of Figure 9A, near focusing ribs 912, follow a serpentine path, rising above focusing ribs 912 and falling above the cavity in which emitters 909 are

located. However, the presence of spacer wall 909 imposes an equipotential line at this location, i.e., the bottom of spacer wall 909, that is straight. According to the invention, one of electrodes 917 can be located near the bottom of spacer wall 909 and formed in a serpentine path in order to create a potential field having equipotential lines with the desired serpentine shape.

Figure 10 is a graph of voltage versus distance 907 (Figure 9B) from field emitters 909. Anode 914 is spaced apart from field emitters 909 by distance 916, and is held at a higher voltage (designated as HV in Figure 10) than field emitters 909. For a group of field emitters 909 that are distant from one of spacer walls 908, e.g., field emitters 909b, spacer walls 908 do not interfere with the flow of electrons 915 from field emitters 909 and the voltage change from field emitters 909 to anode 914 is approximately linear as shown in Figure 10.

It is necessary that the voltage change near each spacer wall 908 also change linearly between field emitters 909 and anode 914, so that the flow of electrons is not distorted (and the display image thereby degraded). However, for a group of a field emitters 909 that are near one of spacer walls 908, e.g., field emitter 909a, the adjacent spacer wall 908 can interfere with the flow of electrons 915 from field emitters 909. Stray electrons 915 emitted from field emitters 909a will strike spacer wall 908, typically resulting in the accumulation of charge on spacer wall 908. For a given electron density (current density j) striking spacer wall 908, an amount of charge equal to $j \cdot (1 - \delta)$ accumulates at the surface of spacer wall 908. For $\delta \neq 1$, the accumulation of charge causes a change in voltage at the surface of spacer wall 908 from the desired voltage, resulting in a non-zero flow of electrons from spacer wall 908. If the conductivity of spacer wall 908 is low, the change in voltage will cause the electron flow near spacer wall 908 to be distorted, resulting in degradation of the image display.

Generally, the deviation of voltage near spacer wall 908 from the desired voltage (based on a linear voltage drop from field emitters 909 to anode 914) is given by the equation:

$$\Delta V = \rho_s \cdot [x \cdot (x-d)/2] \cdot j \cdot (1 - \delta) \qquad (1)$$

where

ΔV = voltage deviation (in volts)

ρ_s = sheet resistance of the surface of the spacer wall (in ohms/□)

x = distance from nearest electrode, $0 < x < d$ (in cm)

d = distance between electrodes (in cm)

j = current density striking the surface of the spacer wall (in amperes)

δ = secondary emission ratio (dimensionless)

The above equation assumes that the current density j strikes spacer wall 908 uniformly and that the sheet resistance ρ_s of spacer wall 908 is uniform. More exactly, equation (1) would account for the dependence of current density j on the position on spacer wall 908, and the dependence of secondary emission ratio δ on the exact voltage at the position on spacer wall 908.

As can be seen from equation (1), the maximum voltage deviation ΔV occurs at the midpoint between two electrodes 917 (i.e., the quantity $[x \cdot (x-d)/2]$ is maximized), and is proportional to the distance between the electrodes squared. For this reason, providing additional electrodes 917 minimizes the voltage deviation near spacer wall 908 and, thus, the distortion of the flow of electrons 915 toward faceplate 902. The addition of n electrodes of w to a spacer wall 908 of height h reduces the power consumption of flat panel display 900 according to the ratio given below:

$$\frac{P_{NEW}}{P_{OLD}} = \frac{d - nw}{d \cdot (n + 1)^2} \qquad (2)$$

For example, the addition of four electrodes, each electrode being 4 mils wide, to a spacer wall 908 having a height h of 100 mils reduces the I^2R power loss for a given ΔV_{max} by a factor of approximately 30.

This more efficient charge bleed-off allows a higher value of sheet resistance ρ_s and significant savings in power consumption. Another advantage is that if electrodes 917 protrude slightly, electrodes 917 will intercept much of the charge, preventing the charge from striking the high resistance sections which hold off the voltage. However, each additional electrode 917 increases the manufacturing cost of display 900. The number of electrodes 917 included in flat panel display 900 is chosen as a trade-off between the aforementioned factors.

As further seen in equation (1), for a given number of electrodes 915, the voltage deviation ΔV also decreases as the sheet resistance ρ_s decreases, and as the secondary emission ratio δ approaches 1. Thus, it is desirable that the surfaces of spacer walls 908 have a low sheet resistance ρ_s and a secondary emission ratio δ that approaches 1. Since the secondary emission ratio δ can only go as low as zero, but can increase to a very high number, the secondary emission ratio requirement is typically stated as a preference for a material having a low value of secondary emission ratio δ.

Figure 11 is a graph of secondary emission ratio δ versus voltage illustrating the characteristics of two materials: material 1101 and material 1102. For most high resistivity materials, such as material 1101, the secondary emission ratio δ is greater than 1 (and frequently much greater) for an energy range between 100 volts to 10,000 volts, resulting in a positively charged surface. As described above with respect to Figure 4, anode 914 is typically maintained at a positive voltage of

1500 - 10,000 volts relative to emitters 909. Further, as described above, spacer walls 908 are preferably made of an electrically insulative (i.e., high resistivity) material. Thus, spacer walls 908 are typically positively charged (and frequently highly positively charged), resulting in distortion of the flow of electrons 917 from emitters 909.

However, material 1102 has a secondary emission ratio δ that, for the voltage range in flat panel display 900, remains near 1. Since the voltage deviation ΔV varies as the quantity $1-\delta$, when the surfaces of spacer walls 908 are made of material 1102, little charge (positive or negative) accumulates on the surfaces of spacer walls 908. Consequently, the presence of spacer walls 908 has little impact on the voltage drop between field emitters 909 and anode 914, and, therefore, the distortion of the flow of electrons 915 due to the presence of spacer walls 908 is minimized.

According to the invention, the surfaces of spacer walls 908 facing into enclosure 901 are treated with a material having a secondary emission ratio δ characteristic that looks much like that of material 1102 in Figure 11. Further, the surface is treated so that the surface resistance will be low relative to the bulk resistivity of spacer wall 908, enabling charge to flow easily from spacer walls 908 to backplate 903 or from faceplate 902, but not so low that there will be high current flow from the high voltage phosphor on faceplate 902 and, thus, large power loss.

In one embodiment of the invention, spacer walls 908 are ceramic and coating 904 is a material having a secondary emission ratio δ less than 4 and a sheet resistance ρ_s between 10^9 and 10^{14} ohms/□. In an additional embodiment, the material used for coating 904 has the above sheet resistance ρ_s and a secondary emission ratio δ less than 2. The coating 904 according to this embodiment is, for instance, chromium oxide, copper oxide, carbon,

titanium oxide, vanadium oxide or a mixture of these materials. In a further embodiment, coating 904 is chromium oxide. Coating 904 has a thickness between 0.05 and 20 μm.

In another embodiment of the invention, coating 904 includes a first coating formed on spacer wall 908 of a material having a sheet resistance ρ_s between 10^9 and 10^{14} ohms/□ without regard to the magnitude of the secondary emission ratio δ. The first coating is then covered by a second coating having a secondary emission ratio δ less than 4 in one embodiment, and less than 2 in another embodiment. The material for the first coating is, for instance, titanium-chromium-oxide, silicon carbide or silicon nitride. The material for the second coating is, for instance, chromium oxide, copper oxide, carbon, titanium oxide, vanadium oxide or a mixture of those materials. The total thickness of coating 904 is between 0.05 and 20 μm.

In yet another embodiment of the invention, spacer walls 908 are surface doped to produce a sheet resistance ρ_s between 10^9 and 10^{14} ohms/□, then covered with coating 904 having a secondary emission ratio δ of less than 4 in one embodiment and less than 2 in another embodiment. The dopant can be, for instance, titanium, iron, manganese or chromium. Coating 904 is, for instance, chromium oxide, copper oxide, carbon, titanium oxide or vanadium oxide, a mixture of those materials. In one embodiment, coating 904 is chromium oxide. Coating 904 has a thickness between 0.05 and 20 μm.

In still another embodiment, spacer walls 908 are surface-doped to a concentration to produce a sheet resistance between 10^9 and 10^{14} ohms/□. The dopant can be, for instance, titanium, iron, manganese or chromium.

In another embodiment of the invention, spacer walls 908 are made of a partially electrically conductive ceramic or glass-ceramic material.

The above-described coating 904 can be formed on spacer wall 908 by any suitable method. For example, coating 904 can be formed according to well-known techniques by, for instance, thermal or plasma-enhanced chemical vapor deposition, sputtering, evaporation, screen printing, roll-on, spraying or dipping. Whatever method is used, it is desirable to form coating 904 with a sheet resistance uniformity of ± 2%. Typically this is done by controlling the thickness of coating 904 within a specified tolerance.

An alternative to coating spacer surfaces is to take advantage of a material contained in the initial ceramic layers which can be made to become slightly conductive in a later firing.

In the above embodiments, treatment of spacer walls to minimize or eliminate charging of the surfaces of the spacer walls is described. In embodiments of the invention including a spacer structure, e.g., spacer structure 608 (Figure 6), the surfaces of holes in the spacer structure through which electrons flow are treated, as described above, to minimize or eliminate charging of those surfaces.

Figures 12A through 12D are cross-sectional views illustrating the interface between a spacer wall, resistive coating, edge metallization and focusing ribs according to various embodiments of the invention. The coating in each embodiment can be one of the coatings described above with respect to Figures 9A, 9B and 9C. In each embodiment, a sharply defined edge metallization/resistive coating interface is formed that is straight and at a constant height above the cathode so that a straight equipotential is defined at the base of the spacer wall along the length of the spacer wall parallel to the backplate. Edge metallization according to the embodiments of the invention described below can be formed on the edge surfaces of the spacer walls by the

techniques described above for formation of resistive coating 904.

In Figure 12A, resistive coating 1204 is formed on side surfaces 1208a of spacer wall 1208. Coating 1204 is formed on side surfaces 1208a so that coating 1204 does not extend beyond the end of side surfaces 1208a. Edge metallization 1206 is formed on end surface 1208b of spacer wall 1208 so that edge metallization 1206 does not extend beyond coating 1204.

In Figure 12B, resistive coating 1214 is formed on side surfaces 1218a and end surface 1218b of spacer wall 1218 to entirely cover spacer wall 1218. Edge metallization 1206 is formed adjacent the portion of coating 1218 formed on end surface 1218b of spacer wall 1218 so that edge metallization 1206 does not extend beyond the edge of coating 1204.

In Figure 12C, resistive coating 1214 is formed on side surfaces 1218a and end surface 1218b of spacer wall 1218 to entirely cover spacer wall 1218. Edge metallization 1216 is formed adjacent the portion of coating 1214 formed on end surface 1218b of spacer wall 1218 such that metallization 1216 overlaps coating 1214 and extends around the corner of coating 1214 to a well-defined height.

In Figure 12D, resistive coating 1204 is formed on side surfaces 1208a of spacer wall 1208, as in Figure 12A, so that coating 1204 does not extend beyond the end of side surfaces 1208a. Edge metallization 1216 is formed adjacent the portion of coating 1204 formed on end surface 1208b of spacer wall 1208 such that metallization 1216 overlaps coating 1204 and extends around the corner of coating 1204 to a well-defined height.

As described above, electrodes 915 are formed at intervals on the surfaces of spacer walls 908 that are exposed within enclosure 901. The voltages at these electrodes 915 are set by a voltage divider. The voltage divider can either be coating 904 or a resistive strip,

outside the active region of display 900, connected to electrically conductive traces extending from each of electrodes 915. In order to achieve the desired voltages on each electrode 915, the voltage divider can be "trimmed" by removing material from the voltage divider at selected locations to increase the resistance at those locations as necessary. The trimming can be done by, for instance, using a laser to ablate material from the voltage divider. Alternatively, material can be removed from selected ones of the electrically conductive traces, e.g., the length of one or more of the traces outside of enclosure 901 can be shortened, extending from a voltage divider outside the enclosure to electrodes 915 to achieve the same effect.

Figures 13A through 13H (collectively "Figure 13"), Figures 14A through 14J (collectively "Figure 14"), Figures 15A through 15J (collectively "Figure 15"), and Figures 16A through 16J (collectively "Figure 16") illustrate four basic process sequences for manufacturing the light-emitting structure in the CRT display of Figure 4A. To facilitate describing these processes, the orientation of the various regions in Figures 13, 14, 15, and 16 is upside down from that in Figure 4A. In the following process description, directional terms such as "upper" and "lower" apply to the directional orientation utilized in Figures 13 through 16.

Beginning with the process sequence shown in Figure 13, the starting point is faceplate 302. The intended interior surface of faceplate 302--i.e., the upper faceplate surface here--is roughened as indicated in Figure 13A to reduce the reflectivity of the material used to form the black matrix. The roughening step is typically done with a chemical etchant such as a hydrofluoric acid solution, or with a halogen-based plasma etchant.

Slurry 321 of solder glass capable of forming dark non-reflective frit is screen deposited on the upper

surface of faceplate 302 as shown in Figure 13B. Slurry 321 is converted to hardened solder glass layer 322 by firing (i.e., heating) the structure at 400 - 450°C for 1 - 120 minutes. See Figure 13C. Portions of solder glass layer 322 at locations between sites intended for dark ridges 314 are removed by chemical or plasma etching through a suitable photoresist mask (not shown) or by ablation using a suitably programmed laser. Figure 13D illustrates the resulting structure in which ridges 314 are the remainder of solder glass layer 322.

Phosphor stripes 313r, 313g, and 313b are formed on the upper surface of faceplate 302 in the spaces between dark ridges 314 as depicted in Figure 13E. In particular, a slurry of a polymer, a photosynthesizer, and phosphor particles that emit light of one of the three colors of red, green, and blue is deposited on the upper surface of faceplate 302. The portions of the slurry at the intended sites for the phosphor particles of that color are hardened by exposing those slurry portions to actinic radiation using a suitable photoresist mask (not shown). The remainder of the slurry is poured off, and the structure is rinsed. This procedure is then repeated with phosphor particles that produce light of each of the two remaining colors. The structure is dried to complete the fabrication of phosphor stripes 313.

Layer 323 of lacquer is sprayed on phosphors 313 and ridges 314. The upper surface of lacquer layer 323 is smooth as illustrated in Figure 13F. Aluminum is evaporatively deposited on lacquer layer 323 to form light-reflective layer 315. See Figure 13G. The structure is then heated at approximately 450°C for 60 minutes in a partial oxygen atmosphere to burn out lacquer 323. Figure 14H depicts the final structure while. Because lacquer layer 323 had a smooth upper surface, light-reflective aluminum layer 315 ends up with a smooth lower surface.

Moving to Figure 14, the starting point again is faceplate 302 whose upper surface is roughened. See Figure 15A. Layer 325 of a dark non-reflective metal is deposited on the upper surface of faceplate 302 as shown in Figure 14B. Metal layer 325 typically consists of black chrome or niobium having a thickness of 50 - 200 nm.

Thick photoresist layer 326 is formed on metal layer 325 as shown in Figure 14C. Photoresist layer 326 can, for example, consist of a positive photoresist such as Morton EL2026. The photoresist thickness is 25 - 75 μm, typically 50 μm. Photoresist 326 is selectively exposed to actintic radiation and then developed to form channels 327 of approximately the desired width for ridges 314. That is, the channel width is 10 - 50 μm, typically 25 μm. See Figure 14D in which items 326a are the remainder of photoresist 326.

Channels 327 are selectively filled, or nearly filled, with metal to form metal ridges 314d as depicted in Figure 14E. The selective filling is done according to an electrochemical deposition (electroplating) process. Metal ridges 314d may consist of dark or opaque metal. Typically, the ridge metal is chrome or a nickel-iron alloy. Photoresist mask 326a is subsequently removed to produce the structure shown in Figure 14F.

Using metal ridges 314d as a mask, the exposed portions of dark metal layer 325 are removed. Figure 14G illustrates the resulting structure in which dark ridges 314e are the remainder of metal layer 325. Each dark ridge 314e and overlying ridge portion 314d constitute one of dark ridges 314.

Phosphor stripes 313 and light-reflective layer 315 are now created in the manner discussed above in connection with the process of Figure 13. Figure 14H depicts the formation of stripes 313. The deposition of layer 315 over lacquer layer 323 is illustrated in Figure 14I. Figure 14J illustrates the final light-emitting structure after lacquer 323 is burned out.

The starting point for the process sequence of Figure 15 is transparent electrically insulating flat body (or plate) 329 typically consisting of glass of largely uniform composition. See Figure 15A. Patterned layer 330 of a material capable of acting as a sandblast mask is formed on the upper surface of transparent body 329 as shown in Figure 15B. Mask layer 330 can be formed by depositing a blanket layer of the sandblast masking material on body 329 and then removing selected portions of the blanket layer by a masked etch to expose surface portions of body 329.

A selective removal operation is performed to remove portions of transparent body 329 to a specified depth at the areas exposed through mask 330. Figure 15C illustrates the resulting structure in which the remainder of body 329 consists of faceplate 302 and an overlying pattern of ridges 314f. The removal operation is done by sandblasting. Mask 330 may be eroded away during the sandblasting. If any of mask 330 is present at the end of the sandblasting, the remainder of mask 330 is removed as indicated in Figure 15D.

Layer 331 of dark material is screen deposited on the upper surface of the structure. See Figure 15E. The dark material may consist of dark glass or dark metal. Photoresist mask 332 is typically formed on dark layer 331 directly above ridges 314f as shown in Figure 15F. To avoid misalignment, photoresist mask 332 is typically created by using the photomask reticle employed in creating sandblast mask 330 for negative photoresist or a reverse-image mask for positive photoresist.

Dark ridge portions 314g are respectively created above ridges 314f by removing the exposed portions of dark layer 331. Figure 15G depicts the consequent structure after removal of photoresist 332. Each ridge portion 314g and underlying ridge 314f constitute one of dark ridges 314.

The light-emitting structure is finished in the way described above for the process of Figure 14. In particular, phosphor stripes 313 are formed in the spaces between ridges 314 as shown in Figure 15H. Figure 15I shows the deposition of light-reflective layer 315 over lacquer 323. The final structure is shown in Figure 15J after burning out lacquer 323.

In Figure 16, the starting point is again transparent body 329. See Figure 16A. Layer 325 of metal such as chrome is formed along the upper surface of body 329 as shown in Figure 16B. Portions of metal layer 335 are selectively removed using a masked etch. See Figure 16C in which items 335a are the remainder of metal layer 335.

Layer 336 of negative photoresist capable of acting as a sandblast mask is deposited on the upper surface of the structure as depicted in Figure 16D. Photoresist mask 336 is exposed to actinic radiation from the back (or lower) side of transparent body 329. Metal portions 335a serve as a mask to prevent the overlying portions of photoresist 336 from being exposed to the radiation. The unexposed portions of photoresist 336 are removed to create the structure shown in Figure 16E. Items 336a are the remaining portions of photoresist 336.

Using photoresist mask 336a, a selective removal operation is conducted to remove metal portions 335a and underlying portions of body 329 to a specified depth as shown in Figure 16F. The remainder of body 329, constitutes faceplate 302 and an overlying pattern of ridges 314h. The material removal is done by sandblasting. If any of photoresist 336a is present at the end of the sandblasting, the remainder of photoresist 336a is removed to produce the structure of Figure 16G.

Dark metallic ridge portions 314i are formed on ridges 314h in the same way that dark ridge portions 314g are provided on ridges 314f in the process Figure 15. Figure 16H shows the resulting structure in which each dark ridge portion 314i and underlying ridge 314h

constitute one of dark ridges 314. The light-emitting structure is completed in the manner described above for the process of Figure 14. The formation of phosphor stripes 313 is illustrated in Figure 16I. Figure 16J illustrates the placement of light-reflective layer 315 over stripes 313 and ridges 314.

After fabricating the cathode structure for the CRT of Figure 4A according to one of the processes described in Figures 13 through 16, spacer walls 308 and outer walls 304 are appropriately placed between the cathode structure and the light-emitting black-matrix structure while the components of the display are in a chamber pumped down to a pressure below 10^{-7} torr. The display is then sealed at 300-600°C typically 450°C.

Dark ridges 314 soften, as described above, at a temperature in the range of 300-700°C depending on whether they consist of metal, solder glass, or glass. The ridge-softening temperature is typically chosen to be approximately equal to or slightly less than the display-sealing temperature. As a result, spacer walls 308 penetrate slightly into ridges 314 during the sealing process. This compensates for differences in height among walls 308.

If the ridge-softening temperature exceeds the display-sealing temperature, dark ridges 314 can be pre-softened just before the CRT display is sealed. In that case, spacer walls 308 again penetrate slightly into ridges 314 during sealing to compensate for spacer-wall height differences.

While the invention has been described with reference to particular embodiments, this description is solely for the purpose of illustration and is not to be construed as limiting this scope of the invention claimed below. For example, the dark portions of ridges 314 in each of the process sequences of Figures 15 and 16 could be moved from the tops of ridges 314 to their bottoms by providing a layer of dark material on top of transparent body 329 at

the beginning of the process sequence and then deleting the steps involved in forming upper ridge portions 314g or 314i. Additional parallel dark non-reflective ridges could be formed on faceplate 302 so as to extend perpendicular to ridges 314.

Phosphor stripes 313 could be created from thin phosphor films instead of phosphor particles. Light-emissive regions 313 could be implemented with elements other than phosphors (in particle or film form).

A transparent anode that directly adjoins faceplate 302 could be used in place of, or in conjunction with light-reflective layer 315. Such an anode would typically consist of a layer of a transparent electrically conductive material such as indium-tin oxide. Faceplate 302 and, when present, the adjoining transparent anode then constitute a main section of the light-emitting black-matrix structure. Various applications and modifications may thus be made by those skilled in the art without departing from the true scope and spirit of the invention as defined in the appended claims.

We claim:

1. A flat panel device, comprising:

a faceplate;

a backplate connected to the faceplate to form a sealed enclosure;

means for emitting light from the flat panel device;

a spacer situated within the enclosure and supporting the backplate and the faceplate against forces acting in a direction toward the enclosure, wherein surfaces of the spacer within the enclosure are treated to prevent or minimize charge buildup on the spacer surfaces; and

edge metallization situated between an edge surface of the spacer and the backplate such that the edge metallization forms an electrical connection between the spacer and backplate.

2. A device as in Claim 1, further comprising a coating formed on the spacer surfaces, the coating being a material having a secondary emission ratio less than 4 and a sheet resistance between 10^9 and 10^{14} ohms/□.

3. A device as in Claim 2, wherein the coating is selected from the group comprising chromium oxide, copper oxide, carbon, titanium oxide and vanadium oxide.

4. A device as in Claim 2, wherein the coating is chromium oxide.

5. A device as in any of Claims 2 through 4, wherein the coating has thickness between 0.05 and 20 μm.

6. A device as in Claim 1, further comprising:

a first coating formed on the spacer surfaces, the coating being a material having a sheet resistance between 10^9 and 10^{14} ohms/□; and

a second coating formed over the first coating, the second coating being a material having a secondary emission ratio less than 4.

7. A device as in Claim 6, wherein the combined thickness of the first and second coatings is between 0.05 and 20 μm.

8. A device as in Claim 1, wherein spacer surfaces are surface-doped to produce a sheet resistance between 10^9 and 10^{14} ohms/□

9. A device as in Claim 8, wherein the dopant is titanium.

10. A device as in Claims 8 or 9, further comprising a coating formed over the doped spacer surfaces, the coating being a material having a secondary emission ratio δ less than 4.

11. A device as in Claim 10, wherein the wherein the coating is selected from the group comprising chromium oxide, copper oxide, carbon, titanium oxide and vanadium oxide.

12. A device as in Claim 10, wherein the coating is chromium oxide.

13. A device as in any of Claims 1 through 12, wherein the uniformity of the surface resistance of the spacer surfaces is maintained within 2% of a specified nominal value throughout the spacer.

14. A device as in any of Claims 1 through 13, wherein the spacer further comprises a spacer wall.

15. A device as in Claim 1, wherein the spacer further comprises a spacer structure through which a plurality of holes are formed.

16. A device as in Claim 15, further comprising an addressing grid through which a plurality of addressing grid holes are formed and wherein each of the plurality of spacer structure holes is aligned with an addressing grid hole or group of addressing grid holes.

17. A device as in Claim 1, further comprising an electrode formed on a surface of the spacer near an interface of the spacer and backplate, the voltage of the electrode being controlled to achieve a desired voltage distribution in the vicinity of the interface.

18. A device as in Claim 17, wherein the electrode follows a serpentine path with respect to an interior surface of the backplate.

19. A device as in Claim 1, further comprising a plurality of electrodes formed on a surface of the spacer at intervals, the voltage of each electrode being controlled to achieve a desired voltage distribution between the backplate and faceplate.

20. A device as in Claim 19, further comprising a voltage divider that establishes the voltage of each electrode.

21. A device as in Claim 20, wherein the voltage divider further comprises a resistive coating formed on the spacer surface.

22. A device as in Claim 20, wherein material is selectively removed from the voltage divider to establish the desired voltages on the electrodes.

23. A device as in Claim 19, further comprising an electrically conductive trace extending from each electrode to a location outside an active region of the device, wherein material is selectively removed from at least one of the traces to establish the desired voltages on the electrodes.

24. A device as in Claim 1, further comprising second edge metallization situated between a second edge surface of the spacer and the faceplate such that the edge metallization forms an electrical connection between the spacer and faceplate.

25. A device as in Claim 24, wherein a resistive coating is formed on the spacer surfaces, the edge metallization being electrically connected to the resistive coating.

26. A device as in Claim 25, wherein the interface between the edge metallization and the resistive coating is at a constant distance from an interior surface of the backplate.

27. A flat panel device comprising:

a faceplate;

a backplate connected to the faceplate to form a sealed enclosure;

means for emitting light from the flat panel device; and

a spacer situated within the enclosure and supporting the backplate and the faceplate against forces acting in a direction toward the enclosure, wherein the spacer is made of ceramic, glass-ceramic, ceramic reinforced glass, devitrifying glass, or metal coated with an insulating layer.

28. A device as in Claim 29 wherein the spacer comprises a spacer wall.

29. A flat panel device comprising:

a faceplate;

a backplate connected to the faceplate to form a sealed enclosure;

means for emitting light from the flat panel device; and

a spacer structure situated within the enclosure and supporting the backplate and the faceplate against forces acting in a direction toward the enclosure, a plurality of spacer structure holes being formed through the spacer structure.

30. A device as in any of Claims 1 through 29, wherein the means for emitting light further comprises:

a field emitter cathode; and

a light emissive structure formed over the faceplate.

31. A method for assembling a flat panel device, comprising the steps of:

mounting a ceramic or glass-ceramic spacer between a backplate and faceplate;

sealing the backplate and faceplate together to encase the spacer in an enclosure.

32. A method as in Claim 31, further comprising the step of mounting an addressing grid within the enclosure, a plurality of addressing grid holes being formed in the addressing grid.

33. A method as in Claim 31 or 32, wherein the spacer comprises a spacer wall.

34. A method as in Claim 33, further comprising the step of aligning the spacer wall.

35. A method as in Claim 34, wherein the aligning step further comprises the steps of:

forming a notch in the addressing grid; and

placing the spacer wall in the notch.

36. A method as in Claim 34, wherein:

the sealing step further comprises the step of attaching a top wall, bottom wall and two side walls between the faceplate and backplate; and

the aligning step further comprises the steps of:

forming a notch in the top wall or the bottom wall, and

placing the spacer wall in the notch.

37. A method as in Claim 31 or 32, wherein the spacer comprises a spacer structure.

38. A method as in Claim 37, further comprising the steps of:

drilling holes in sheets of ceramic or glass-ceramic material; and

attaching the sheets of ceramic or glass-ceramic material together to form the spacer structure.

39. A method for assembling a flat panel device, comprising the steps of:

mounting a spacer between a backplate and faceplate;

treating surfaces of the spacer to prevent or minimize charge buildup on the spacer surfaces;

coating an edge surface of the spacer with edge metallization such that the edge metallization forms

an electrical connection between the spacer and backplate; and

sealing the backplate and faceplate together to encase the spacer in an enclosure.

40. A method as in Claim 39, wherein the step of treating further comprises the step of forming a resistive coating on the spacer surfaces.

41. A method as in Claim 40, wherein the resistive coating is made of chromium oxide.

42. A method as in Claim 40, wherein the resistive coating is formed by chemical vapor deposition.

43. A method as in Claim 40, wherein the resistive coating is formed by sputtering.

44. A method as in Claim 40, wherein the resistive coating is formed by evaporation.

45. A method as in Claim 39, wherein the step of treating further comprises surface doping the spacer surfaces to a predetermined dopant concentration.

46. A light-emitting structure comprising:

a main section;

a pattern of ridges situated along the main section; and

a plurality of light-emissive regions situated along the main section in spaces between the ridges, light being produced by the light-emissive regions upon being struck by electrons, the ridges being substantially non-emissive of light relative to the light-emissive regions when the ridges are struck by electrons, the ridges extending further away from the main section than the light-emissive regions, each

ridge comprising a dark region that encompasses substantially the entire width of that ridge and at least part of its height.

47. A structure as in Claim 46, wherein at least part of the ridges extend generally parallel to one another.

48. A structure as in Claim 46, wherein the ridges comprise at least two groups extending in different directions.

49. A structure as in any of Claims 46 through 48, wherein the main section comprises a plate which is transparent at least at portions extending along the light-emissive regions.

50. An optical display comprising:

first and second plates having respective interior surfaces that face, and are spaced apart from, each other;

a pattern of ridges situated along the interior surface of the first plate;

a plurality of light-emissive regions situated along the interior surface of the first plate in spaces between the ridges, the first plate being transparent at least in portions extending along the light-emissive regions, the ridges extending further away from the first plate than the light-emissive regions;

an array of laterally separated sets of electron-emissive elements situated along the interior surface of the second plate, light being produced by the light-emissive regions upon receiving electrons from the electron-emissive elements, the ridges being substantially non-emissive of light relative to the light-emissive regions when the

ridges receive electrons from the electron-emissive elements; and

supporting structure that supports the plates and keeps them spaced apart from each other.

51. A display as in Claim 50, wherein each ridge comprises a dark region that encompasses substantially the entire width of that ridge and at least part of its height.

52. A display as in Claim 50 or 51, wherein the supporting structure includes a group of laterally separated internal supports situated between the ridges and the second plate so as to cross the ridges, the internal supports being spaced apart from the light-emissive regions and extending towards areas between the electron-emissive elements.

53. A display as in Claim 51, wherein each internal support comprises a spacer wall.

54. A display as in any of Claims 50 through 53, further including a light-reflective layer situated along the light-emissive regions across from the first plate for reflecting light from the light-emissive regions towards the first plate.

55. A fabrication method comprising the steps of:

creating a dark layer along a main section;

removing selected portions of the dark layer to form a pattern of ridges along the main section; and

providing a plurality of light-emissive regions along the main section in spaces between the ridges such that the ridges extend further away from the main section than the light-emissive regions.

56. A method as in Claim 55, wherein the dark layer comprises glass.

57. A fabrication method comprising the steps of:

creating a layer of first metal along a main section;

forming a mask over the layer of first metal;

electrochemically depositing portions of second metal into openings in the mask to form a pattern of ridges of the second metal;

removing the mask; and

providing a plurality of light-emissive regions in spaces between the ridges such that the ridges extend further away from the main section than the light-emissive regions.

58. A method as in Claim 57, further including the step of removing portions of the first metal not covered by the portions of the second metal to extend the ridges to include remaining portions of the second metal.

59. A method as in Claim 57 or 58, wherein at least one of the first and second metals is dark metal.

60. A fabrication method comprising the steps of:

selectively removing portions of a body of largely uniform composition to a specified depth such that the remainder of the body comprises a main section and a pattern of ridges that overlie the main section at sites between the removed portions of the body; and

providing a plurality of light-emissive regions along the main section in spaces between the ridges such that the ridges extend further away from the main section than the light-emissive regions.

61. A method as in Claim 60, wherein the removing step entails attacking the body through a mask.

62. A method as in Claim 60, wherein the removing step comprises:

furnishing an initial patterned layer along the body such that openings extend through the initial layer at intended sites for the ridges;

subsequently forming a pattern of masking material in the openings through the initial layer;

removing the initial layer; and

attacking the body through openings in the pattern of masking material.

63. A method as in Claim 62, wherein the forming step comprises:

providing a layer of the masking material over the initial layer and in the openings through it;

selectively exposing the layer of the masking material to backside actinic radiation that passes largely through the body using the initial layer to substantially prevent overlying portions of the masking material from being exposed to the radiation; and

substantially removing portions of the masking material not exposed to the radiation.

64. A method as in any of Claims 61 through 63, wherein the attacking step is performed by sandblasting.

65. A method as in any of Claims 60 through 64, further including the step of forming a pattern of dark portions respectively covering the ridges.

66. A method as in any of Claims 55 through 65, wherein light is produced by the light-emissive regions when electrons strike them, and the ridges are

substantially non-emissive of light relative to the light-emissive regions when electrons strike the ridges.

67. A method as in any of Claims 55 through 66, further including the step of creating a light-reflective layer along the light-emissive regions across from the main section.

68. A method as in any of Claims 55 through 67, wherein the main section comprises a plate which is transparent at least at portions extending along the light-emissive regions.

69. A method as in any of Claims 55 through 68, wherein the ridges soften when they are raised to a temperature in the range of 300 - 700°C.

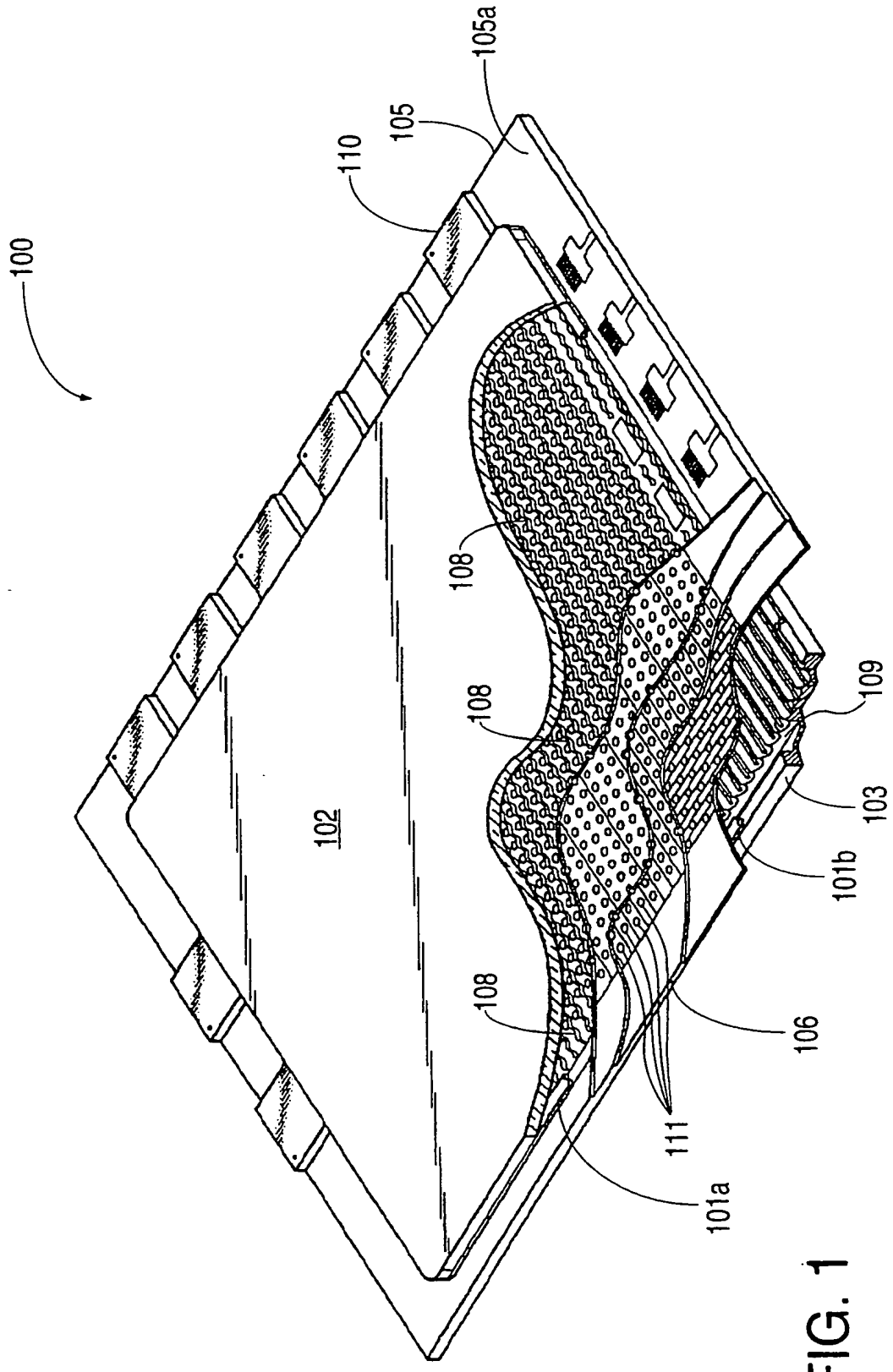


FIG. 1

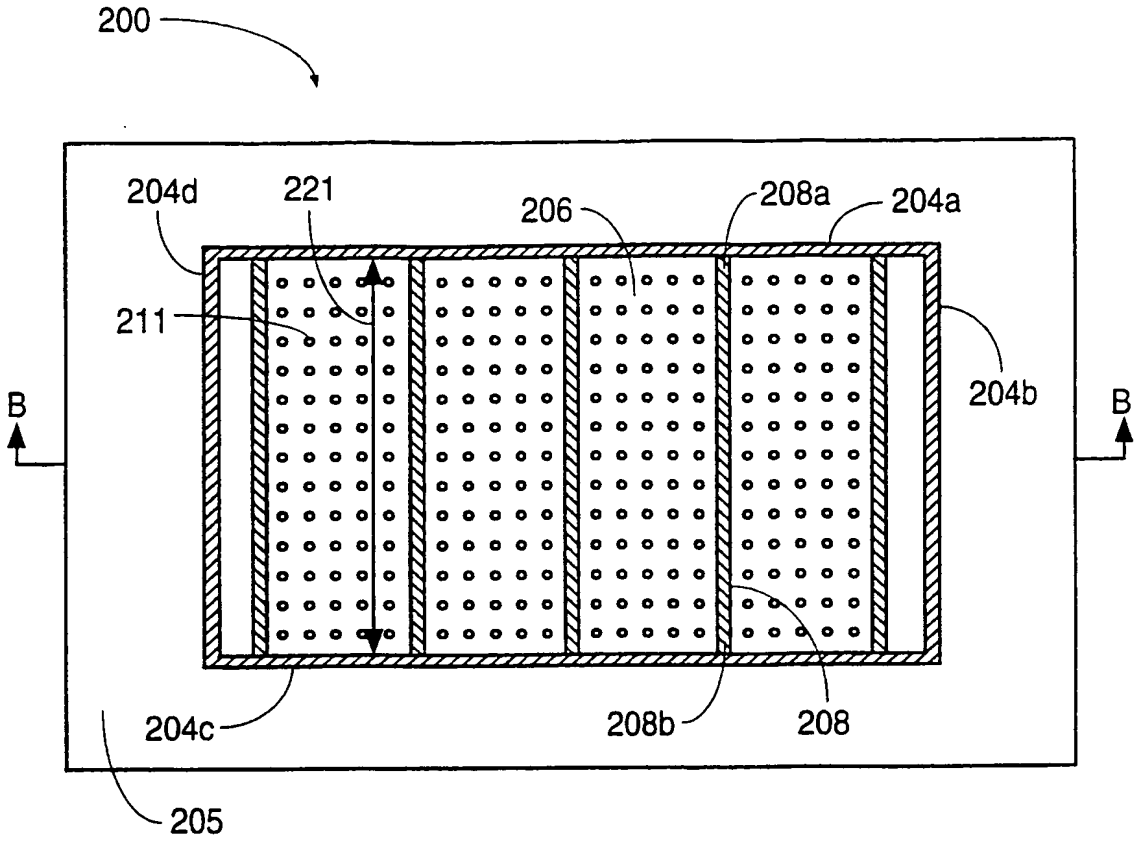


FIG. 2B

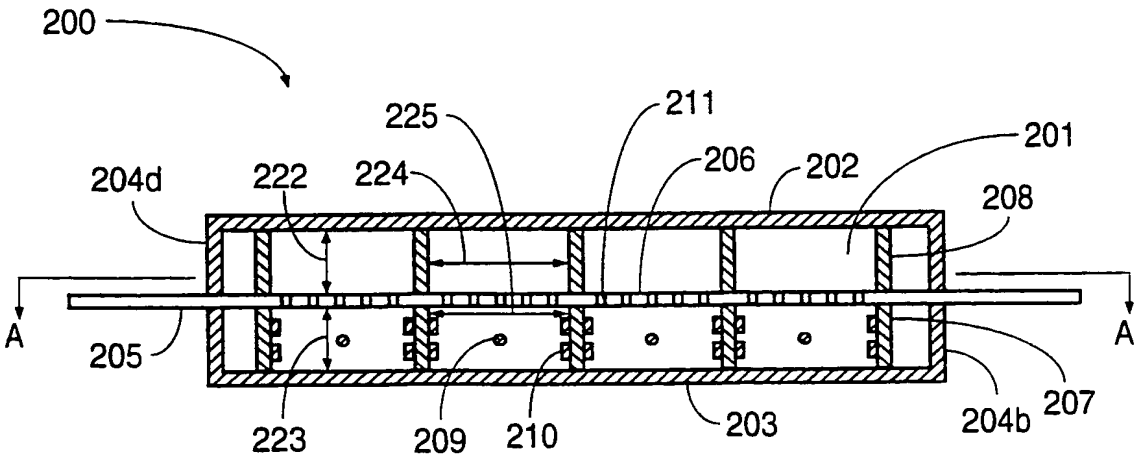


FIG. 2A

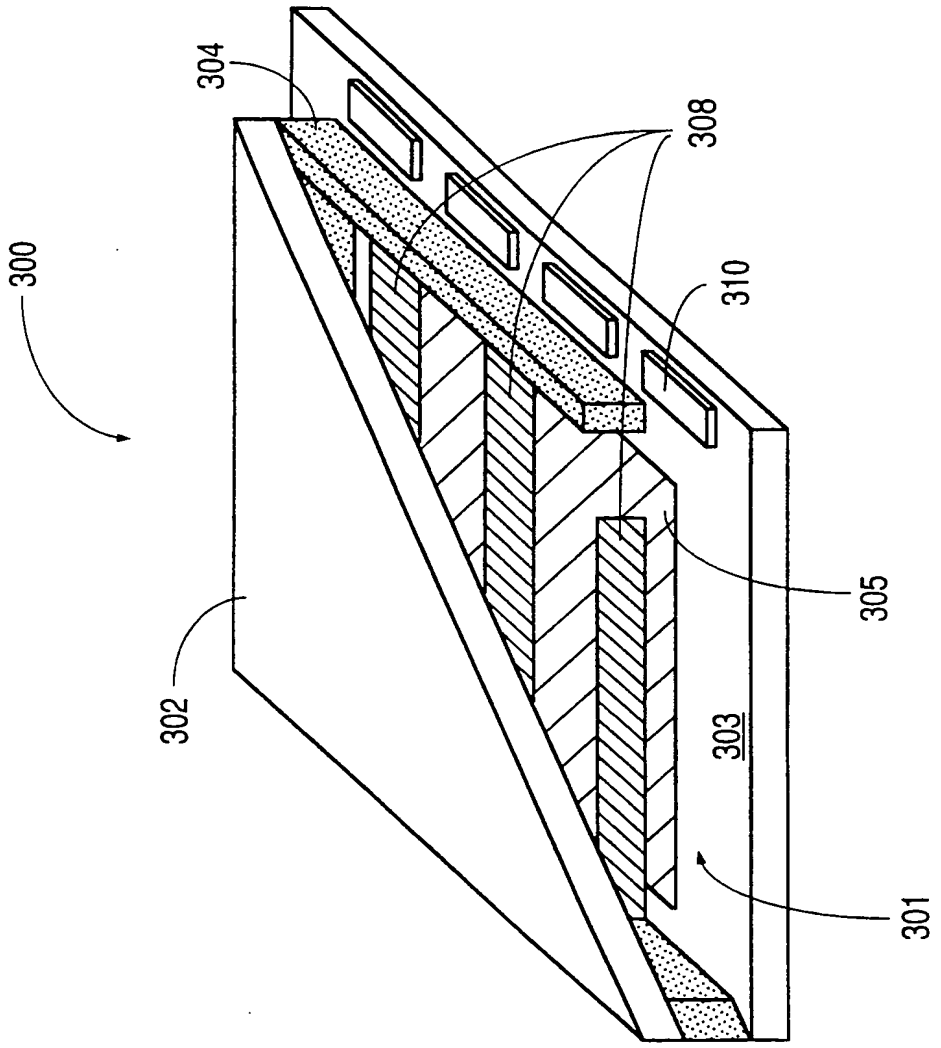


FIG. 3

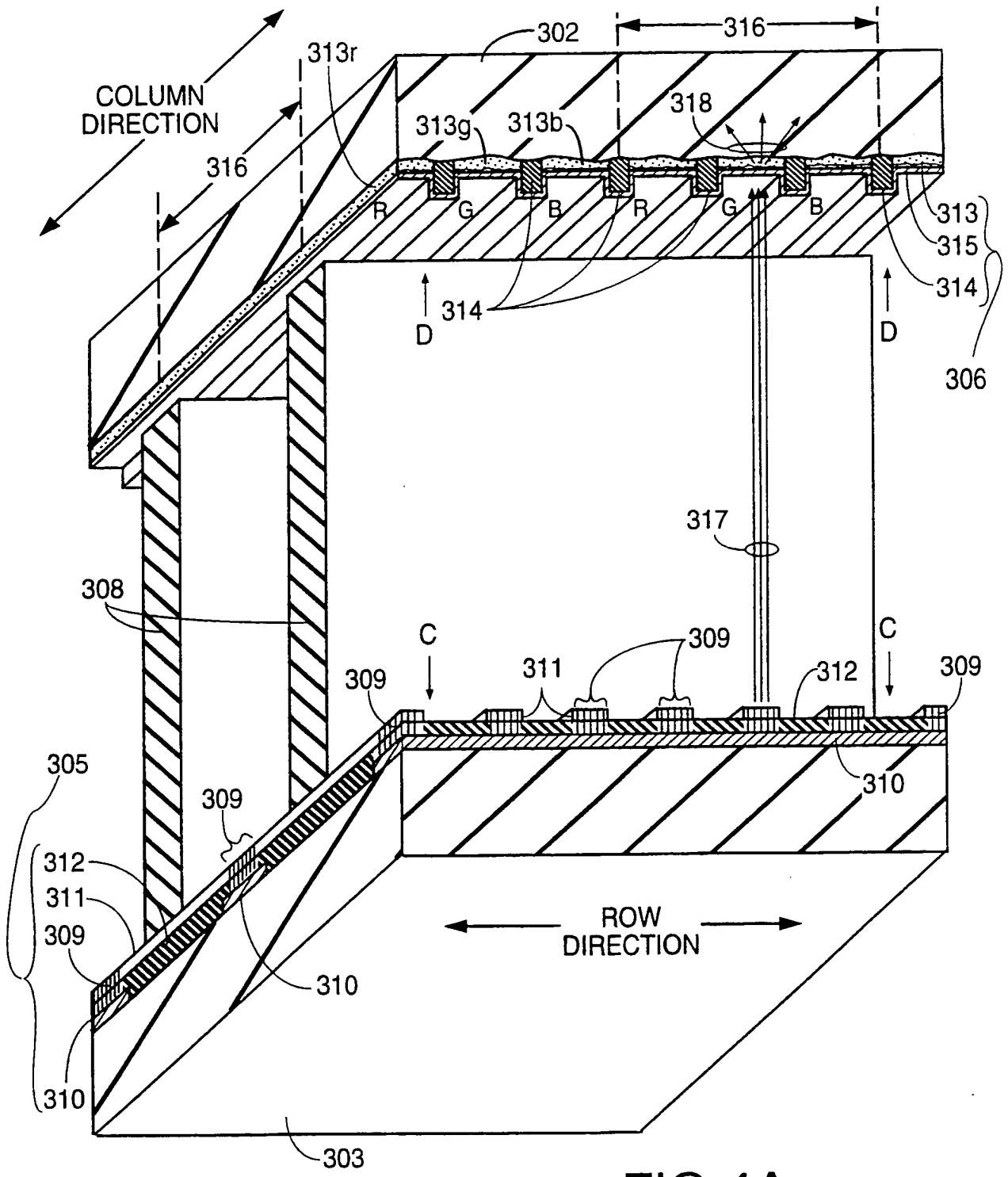


FIG.4A

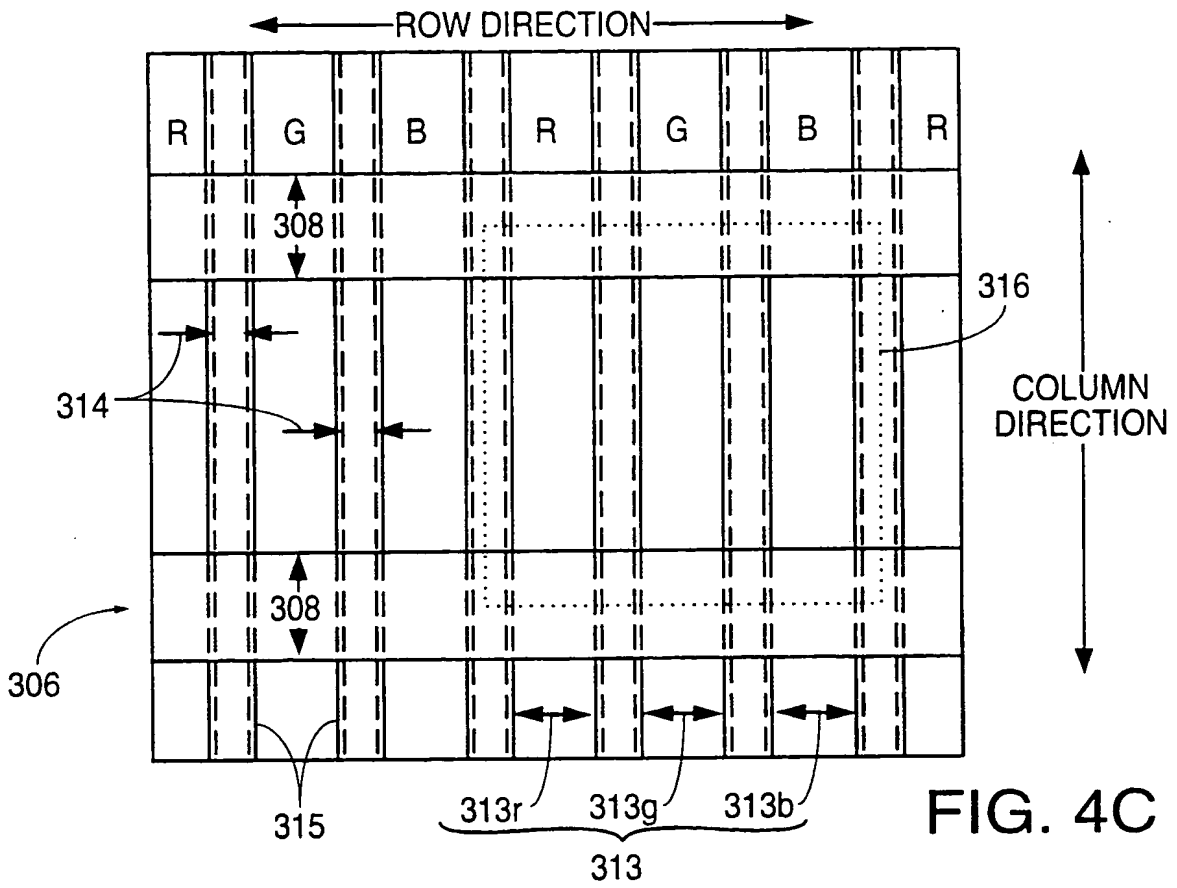


FIG. 4C

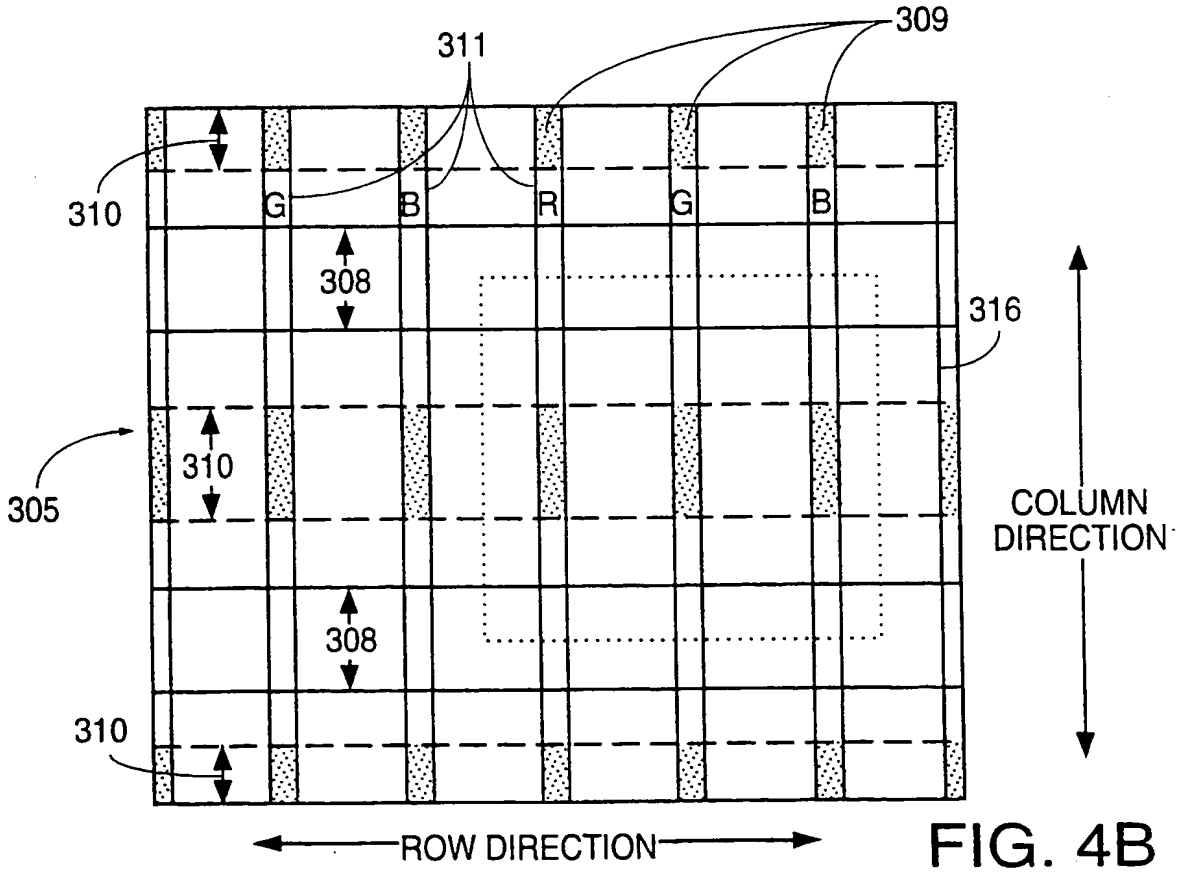


FIG. 4B

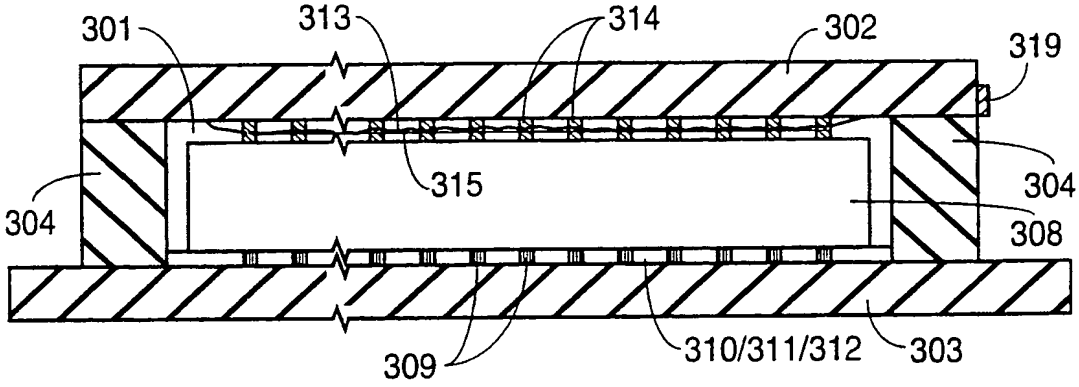


FIG. 4D

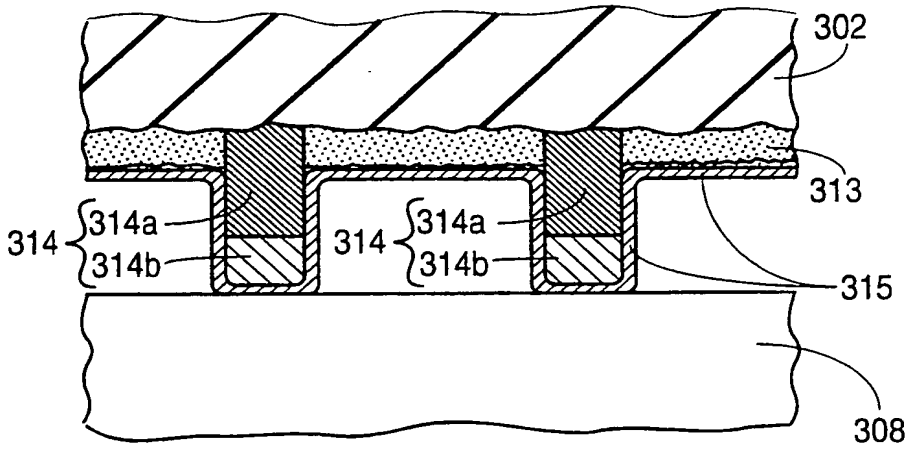


FIG. 4E

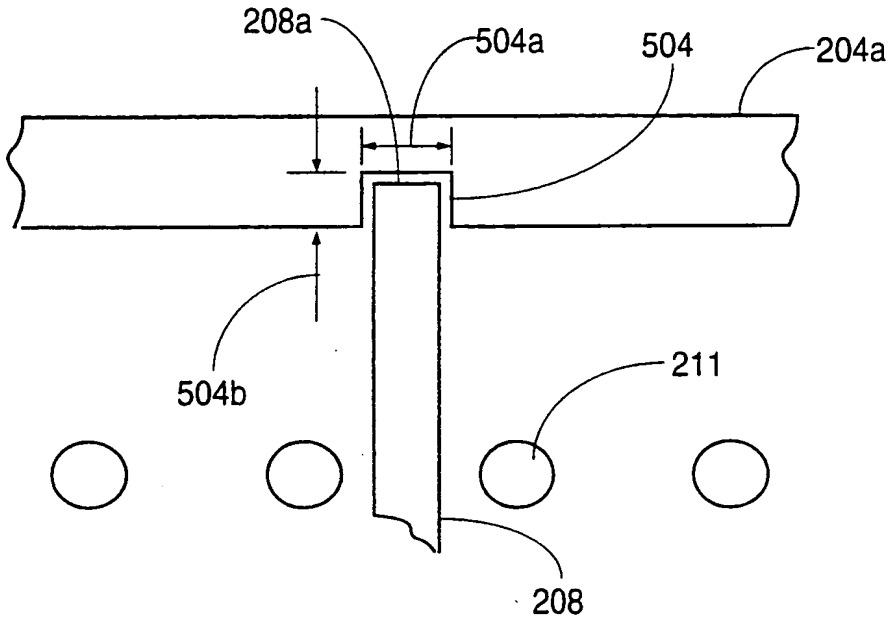


FIG. 5

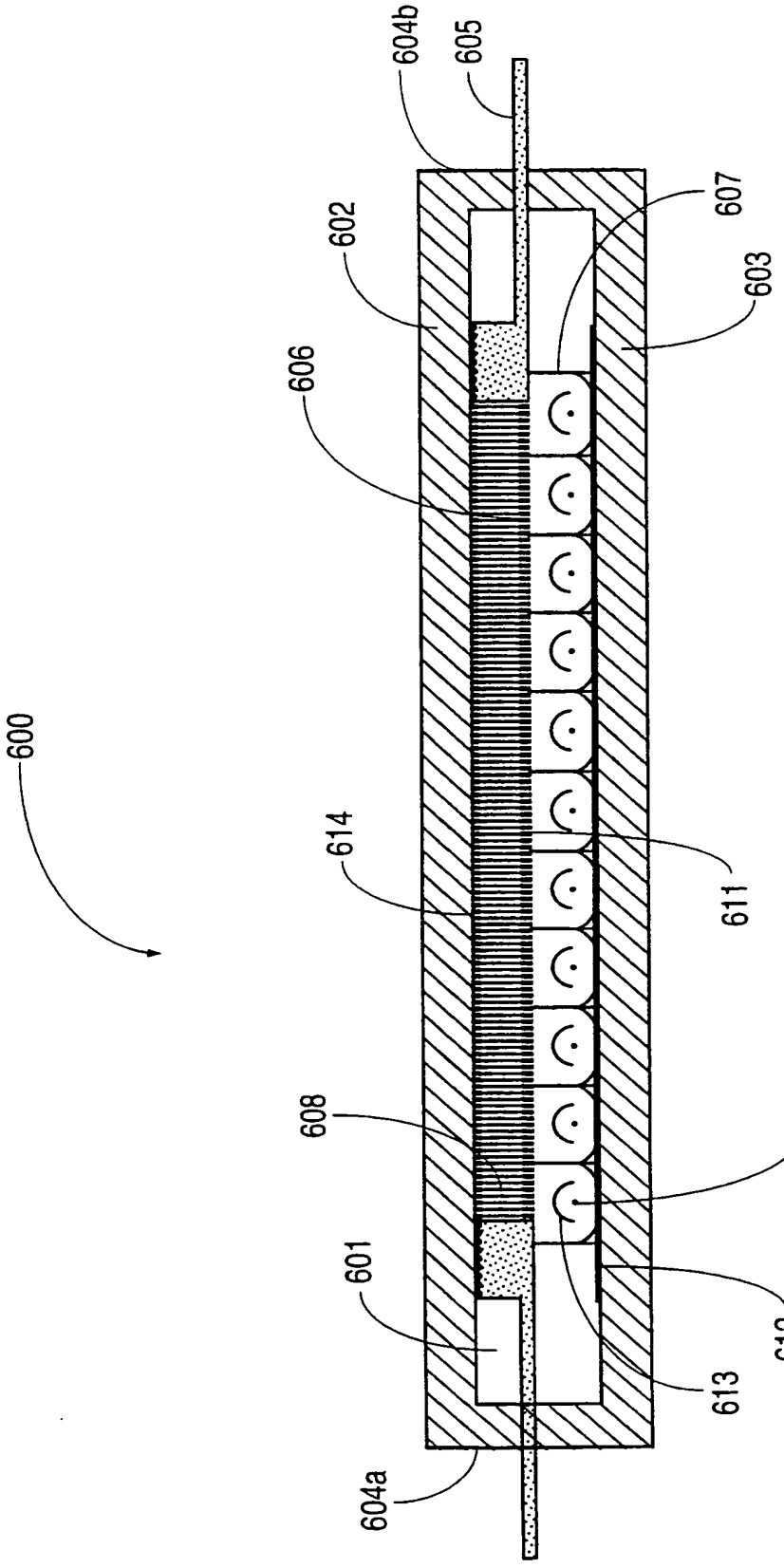


FIG. 6

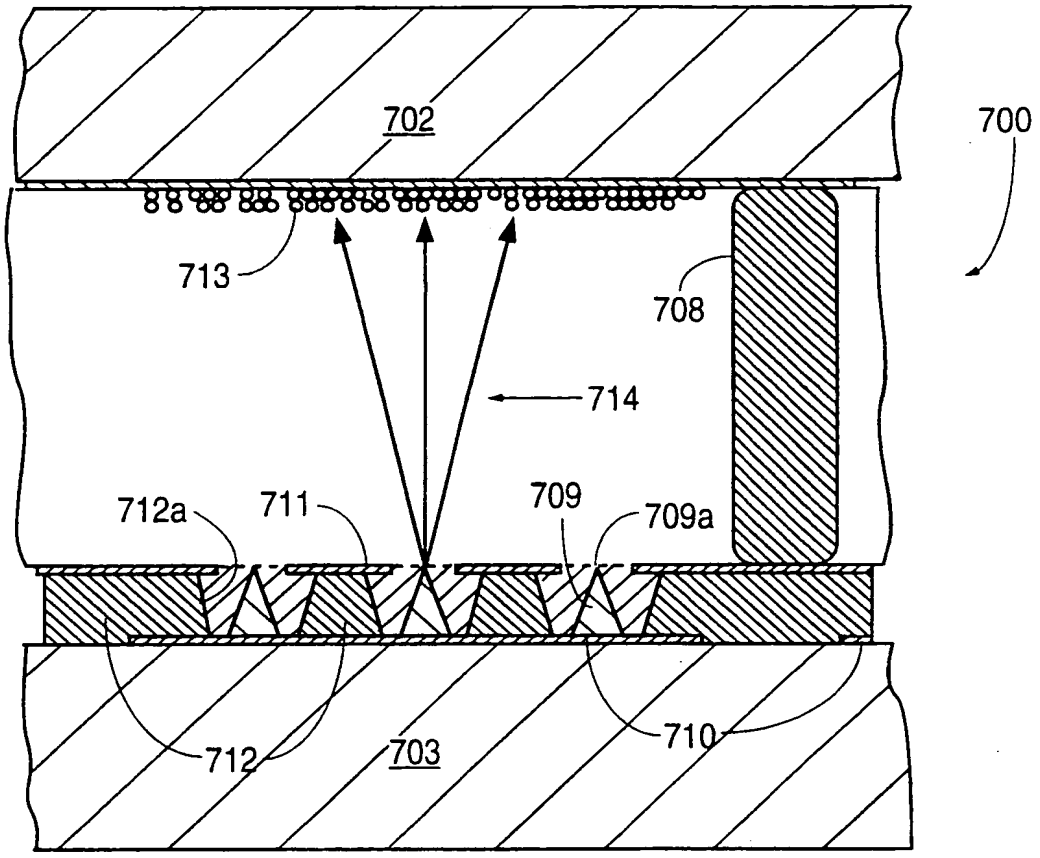


FIG. 7A

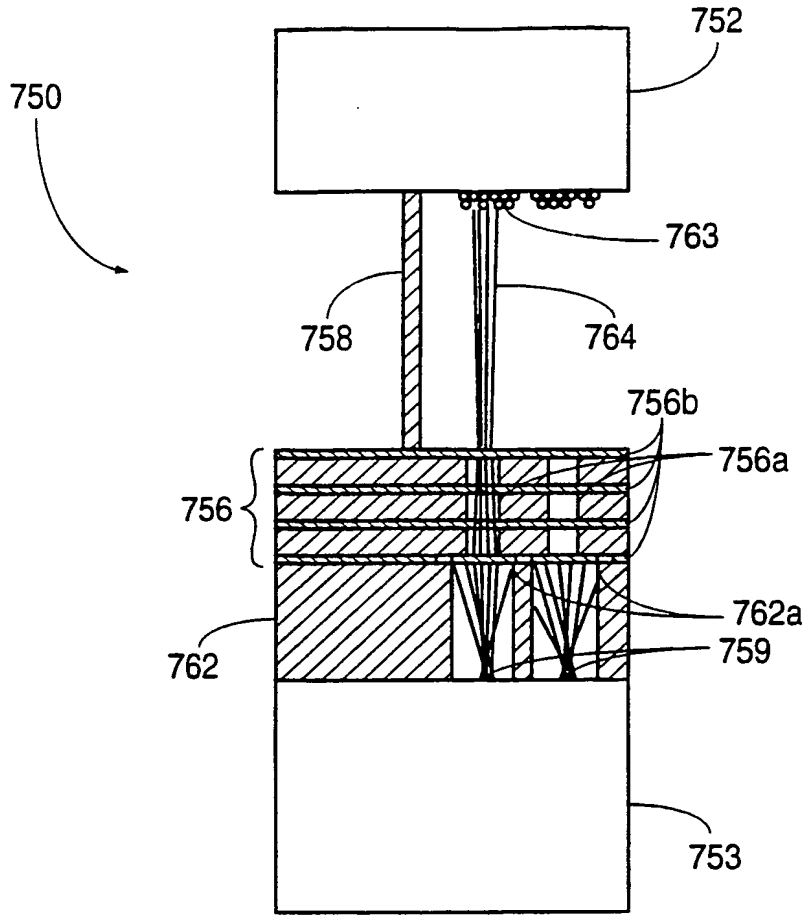


FIG. 7B

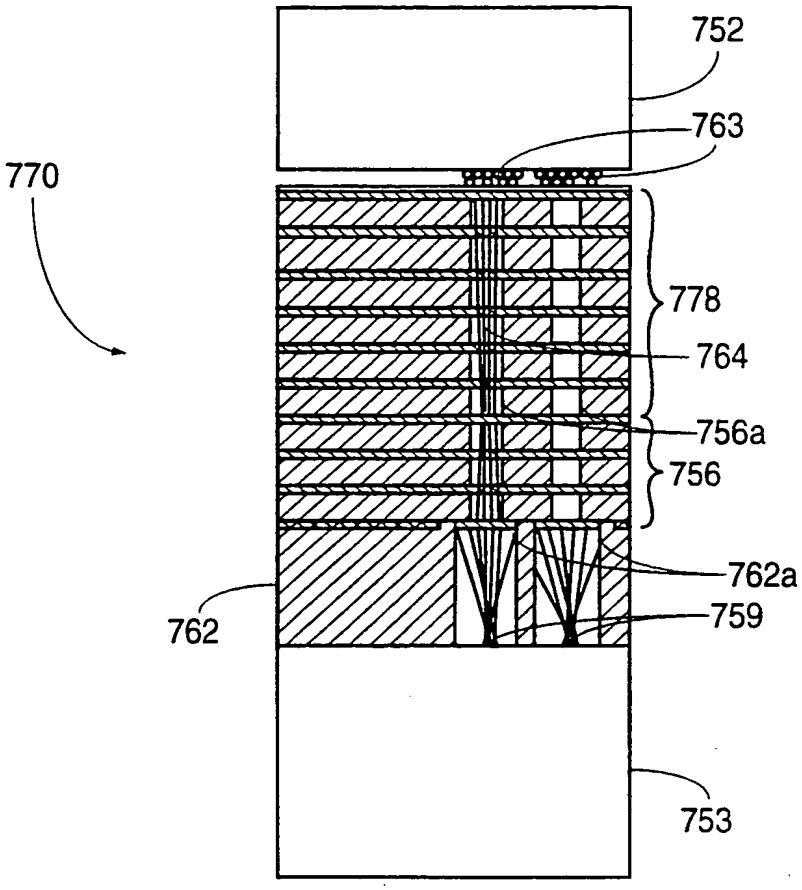


FIG. 7C

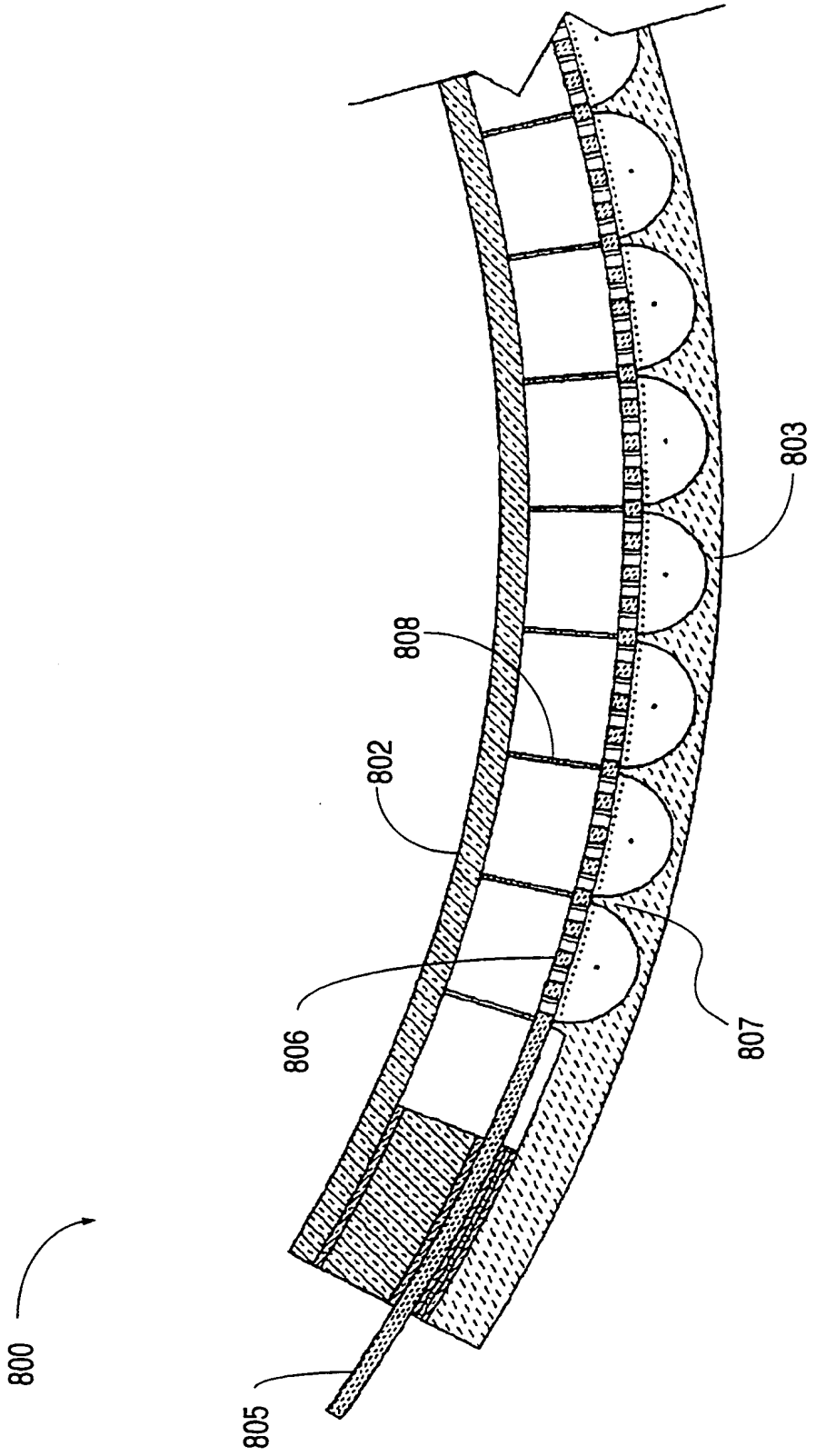


FIG. 8

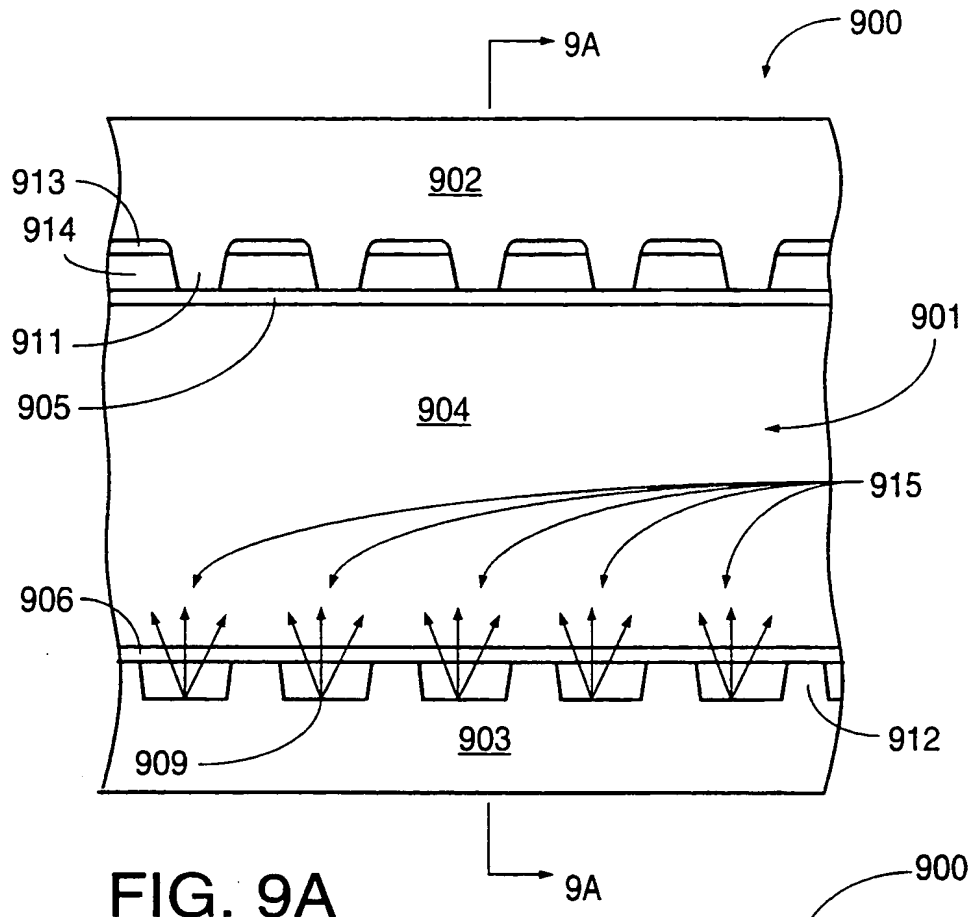


FIG. 9A

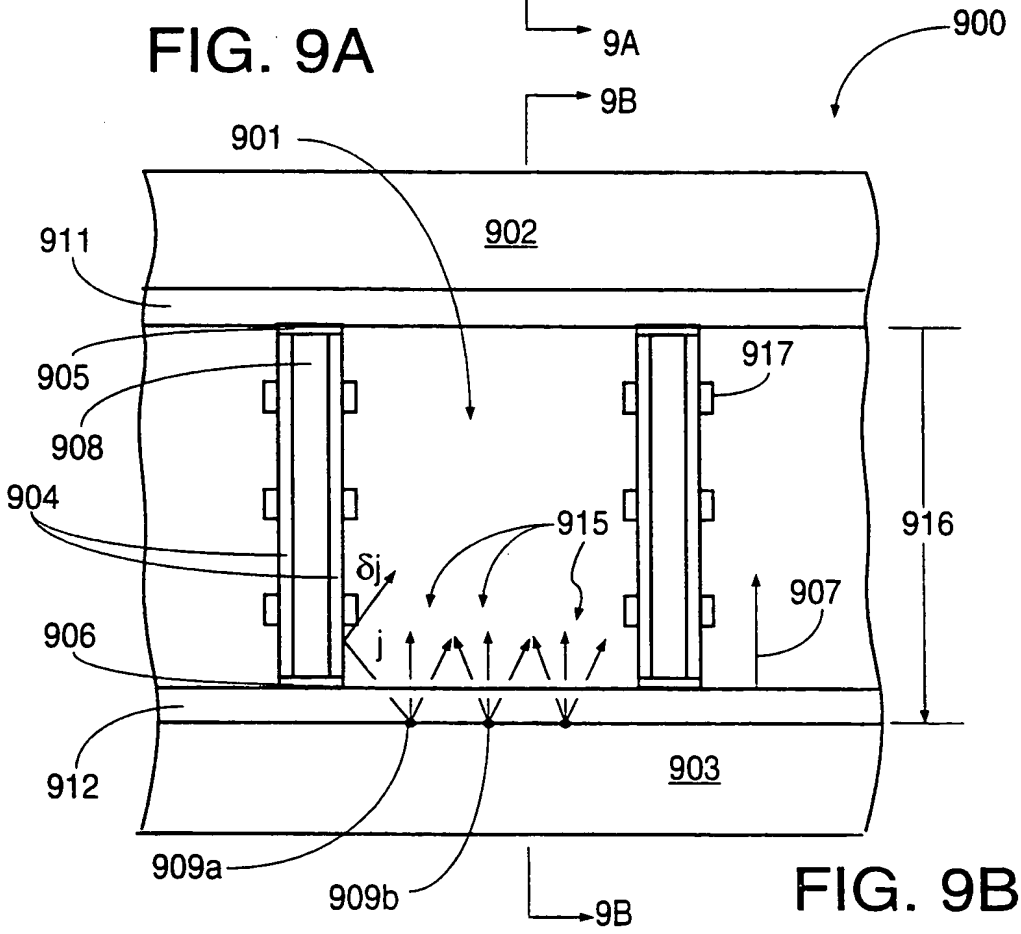


FIG. 9B

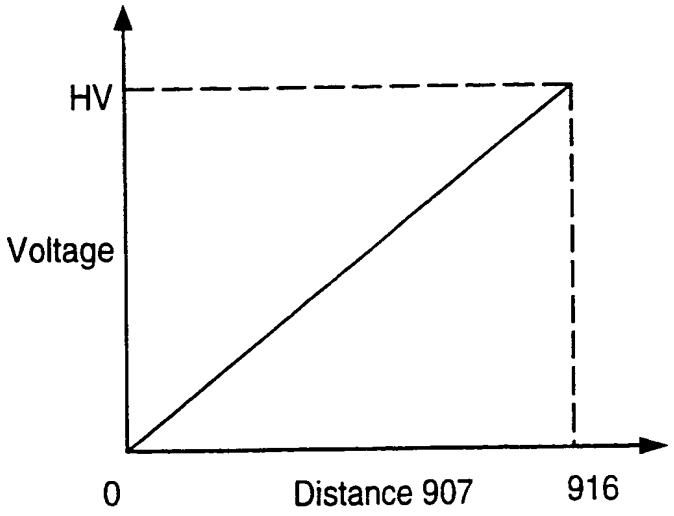


FIG. 10

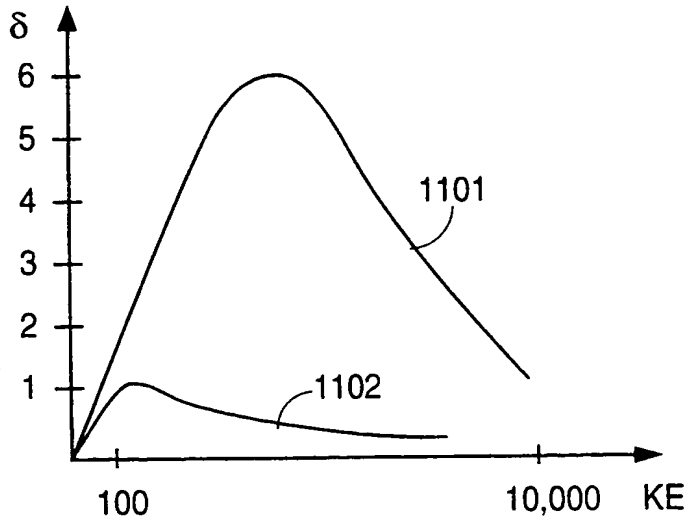


FIG. 11

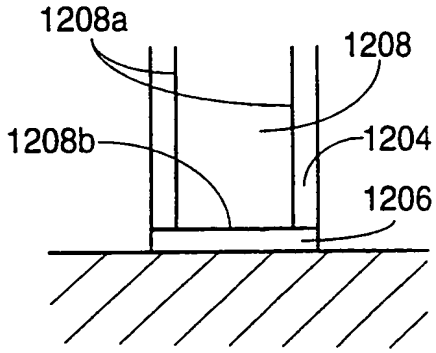


FIG. 12A

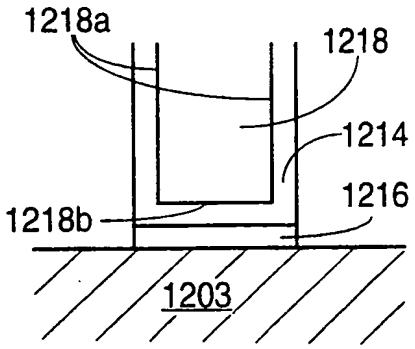


FIG. 12B

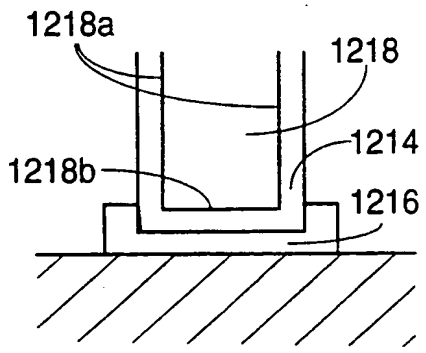


FIG. 12C

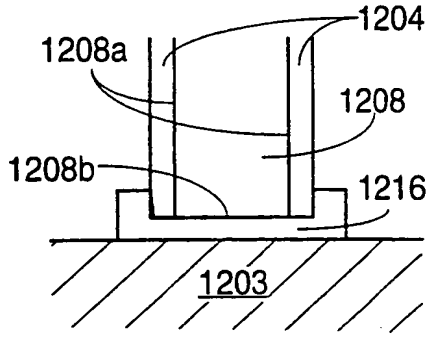


FIG. 12D

FIG. 13A

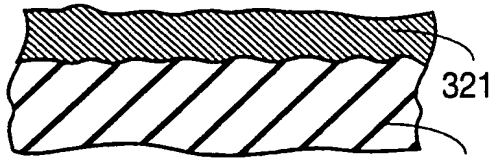


FIG. 13B

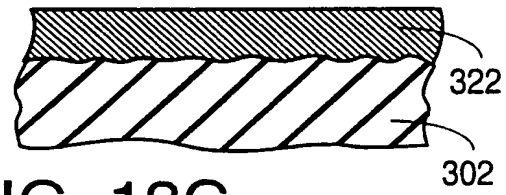


FIG. 13C

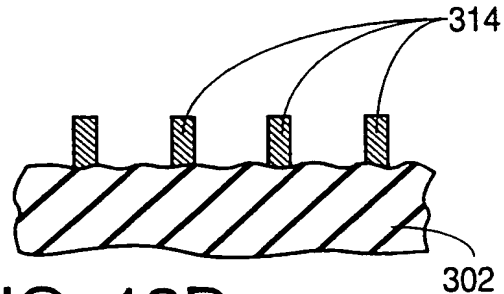


FIG. 13D

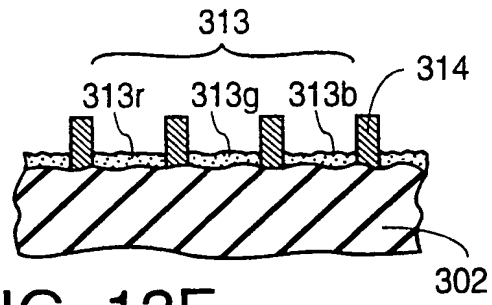


FIG. 13E

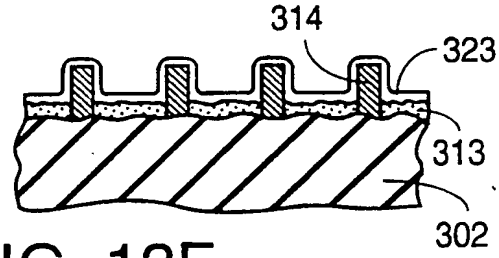


FIG. 13F

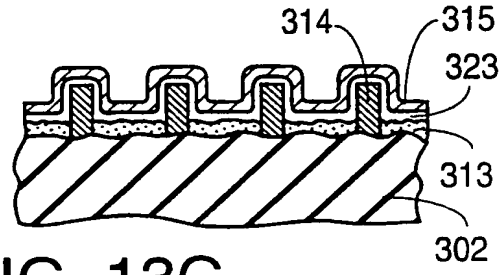


FIG. 13G

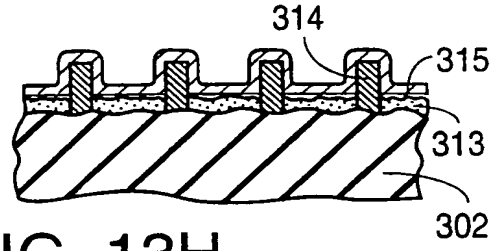


FIG. 13H

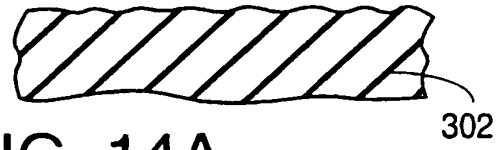


FIG. 14A

FIG. 14B

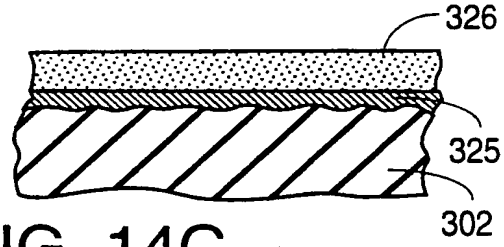


FIG. 14C

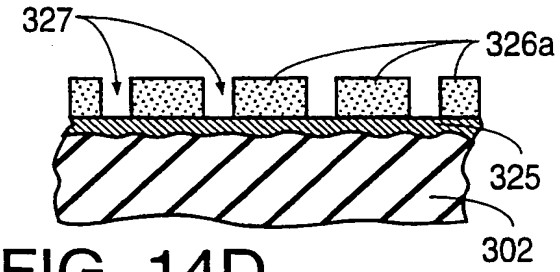


FIG. 14D

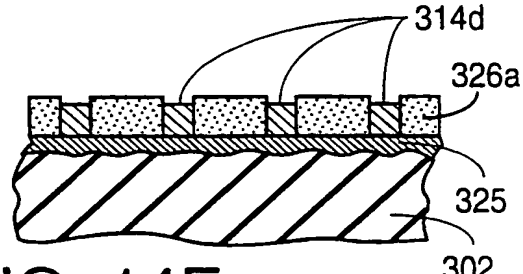


FIG. 14E

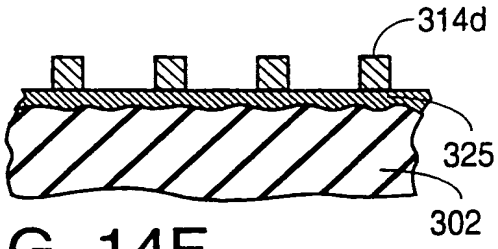


FIG. 14F

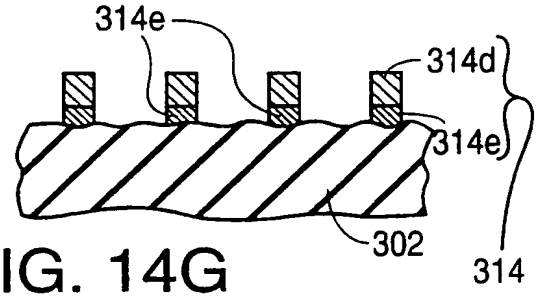


FIG. 14G

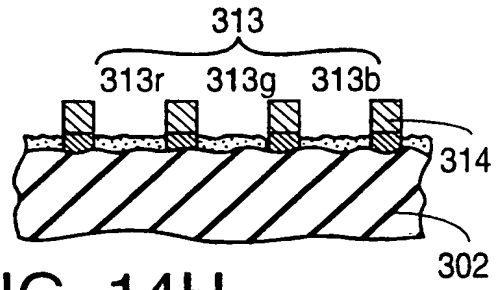


FIG. 14H

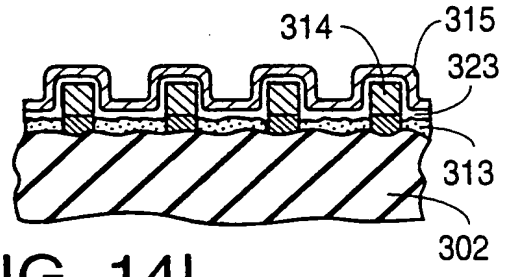


FIG. 14I

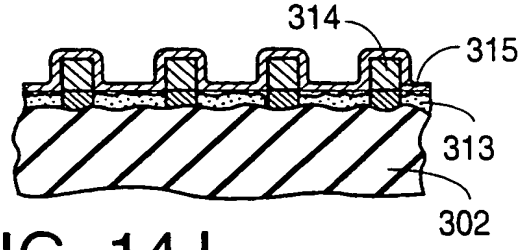


FIG. 14J

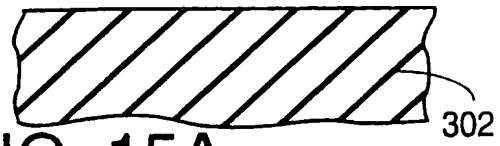


FIG. 15A

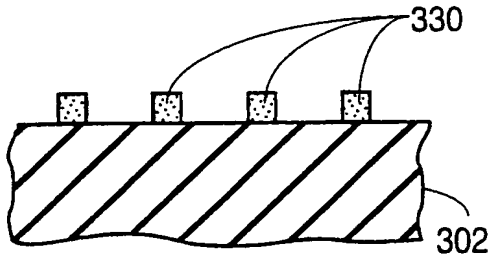


FIG. 15B

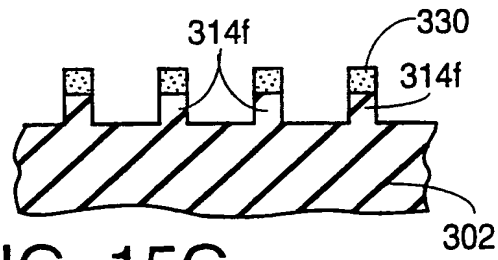


FIG. 15C

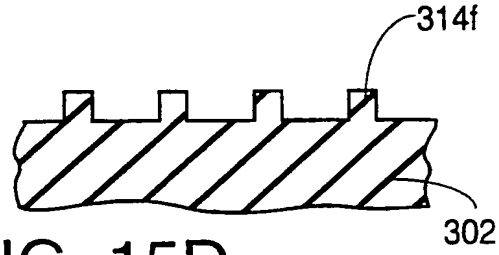


FIG. 15D

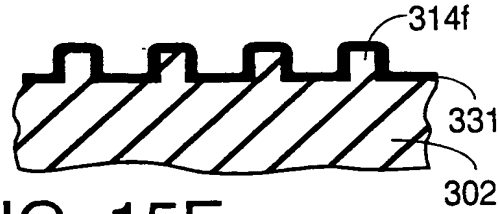


FIG. 15E

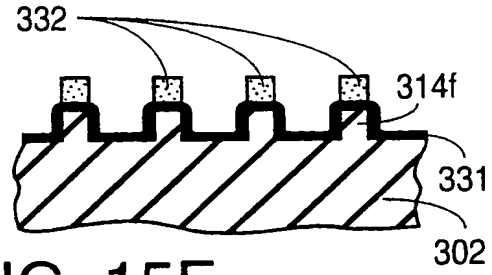


FIG. 15F

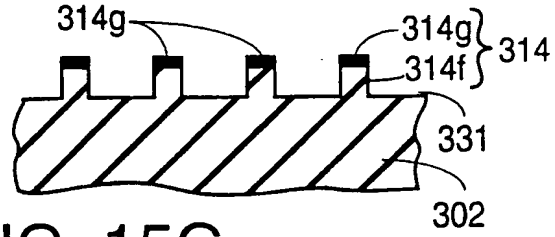


FIG. 15G

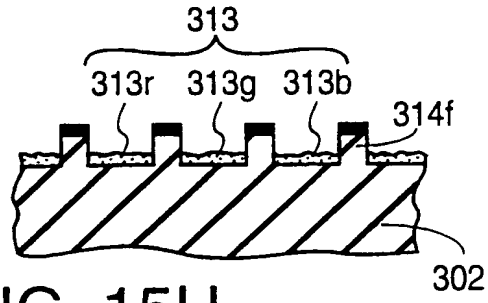


FIG. 15H

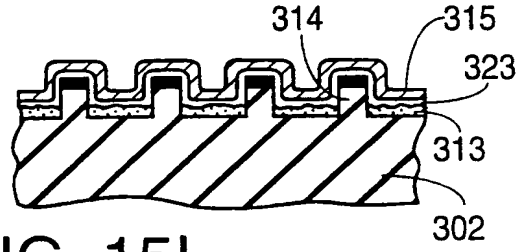


FIG. 15I

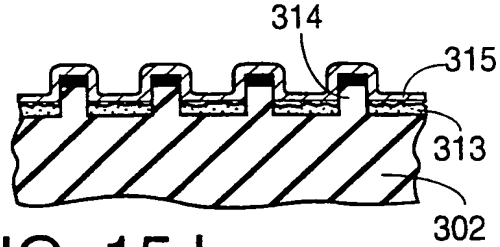


FIG. 15J

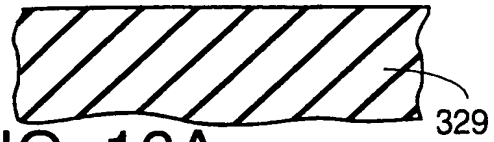


FIG. 16A

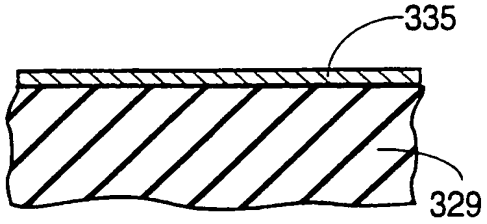


FIG. 16B

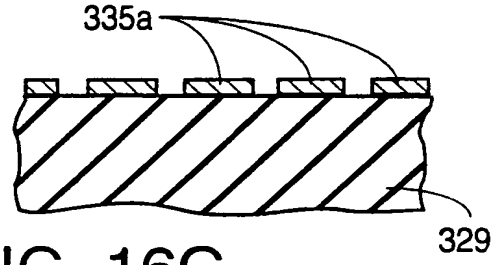


FIG. 16C

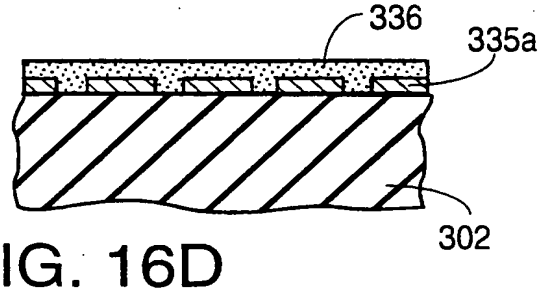


FIG. 16D

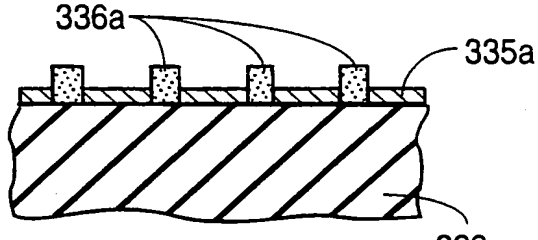


FIG. 16E

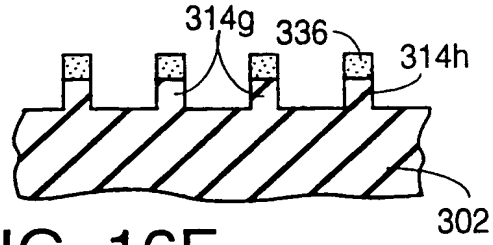


FIG. 16F

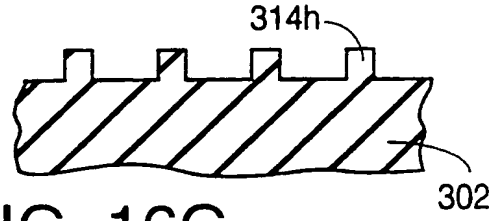


FIG. 16G

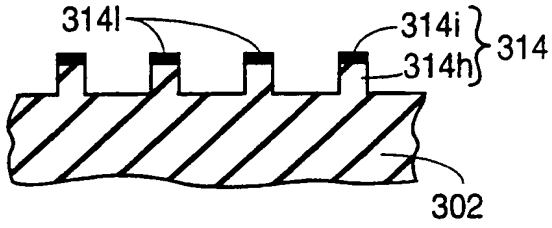


FIG. 16H

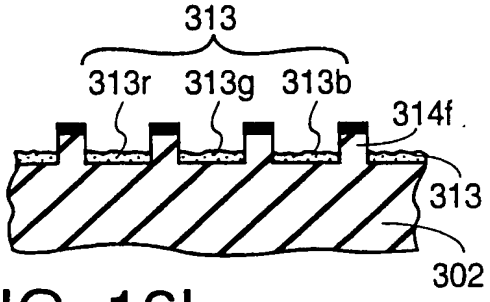


FIG. 16I

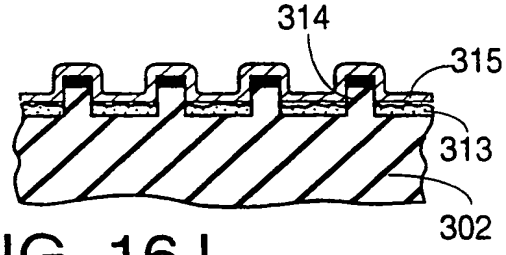


FIG. 16J

INTERNATIONAL SEARCH REPORT

Int. tional application No.
PCT/US94/00602

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01J 63/02; H01J 9/26
US CL :313/422; 445/22; 430/321

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A Y	US, A, 5,063,327 (BRODIE ET AL) 05 November 1991, Figure 4, column 4, line 61-column 5, line 39.	1 27, 28 and 30
Y	US, A, 5,160,871 (TOMII ET AL) 03 November 1992, Figures 8-10, column 8, line 49-column 9, line 8.	27, 28 and 30.
X	US, A, 5,003,219 (MURAGISHI ET AL) 26 March 1991, Figures 1, 7 and 12, column 4, lines 29-51, column 6, lines 29-35.	27, 28, 30-34 and 37.

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 06 MAY 1994	Date of mailing of the international search report JUN 27 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer ASHOK PATEL Telephone No. (703) 305-4934

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

Int. ional application No.
PCT/US94/00602

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,857,799 (SPINDT ET AL) 15 August 1989, Figures 2, 3 and 5, column 3, line 3-column 4, line 64.	1
Y		27, 28, 30, 31, 33 and 34

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*

B. FIELDS SEARCHED
Minimum documentation searched
Classification System: U.S.

313/422, 495, 497, 444, 485, 577, 292, 312, 317; 445/22, 25; 156/663, 655, 656, 315/169.4; 348/796, 797; 345/41, 37, 50; 430/311, 314, 320, 321

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

Group I: Claims 1-45 and 50-54, class 313, subclass 422; and class 445, subclass 22.
Group II: Claims 46-49 and 55-69, class 156, subclass 663 and class 430, subclass 311.

Group I is directed to an invention of (1) a flat panel display device including a spacer structure and (2) a method of manufacturing the display device, whereas Group II is directed to an invention of (1) a light emitting structure and an optical device including a structure of ridge(s) and (2) a method of manufacturing the light emitting structure and the optical device.